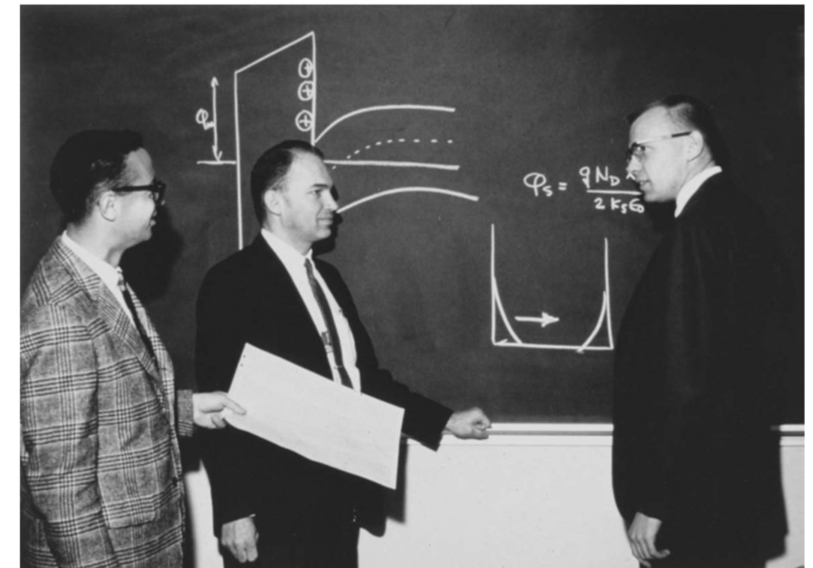
PHYSIQUE DES COMPOSANTS SEMI-CONDUCTEURS

X) FET et MOSFET: partie 1

P.A. Besse

EPFL

A. Grove, B. Deal et Ed. Snow, Fairchild, 1966



“A Company of Legend: The Legacy of Fairchild Semiconductor » David A. Laws, Computer History Museum

PAB

Historique du MOSFET

- **1926 – Concept du FET**

  J. Lilienfeld (US patent)

  …

  …

- **1960 – Premier MOS**

  D. Kahng (US patent)

- **1963 - Invention du CMOS**

  F.M. Wanlass et C.T. Sah

- **1964 – Premier MOS IC commercial**

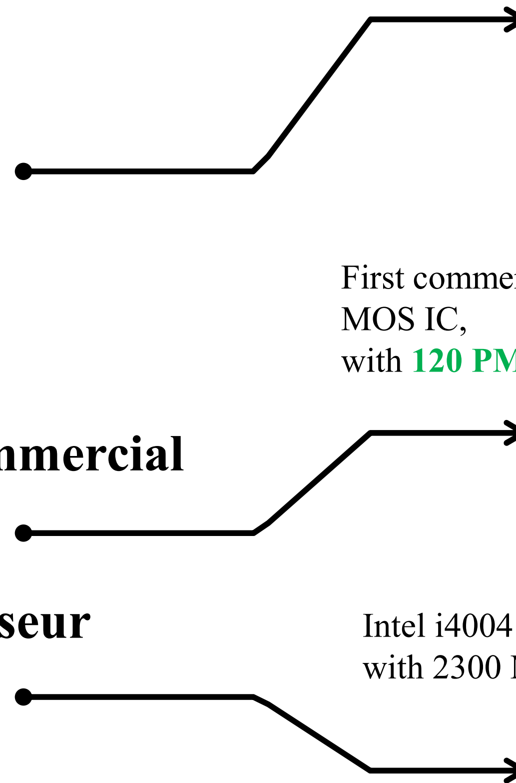
  General Microelectronics

- **1971 – Premier microprocesseur**

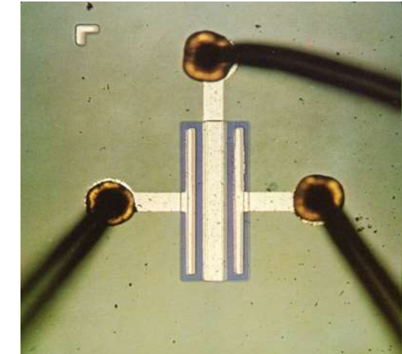
  Intel i4004: 2300 transistors

- **2007 – Intel Itanium 2**

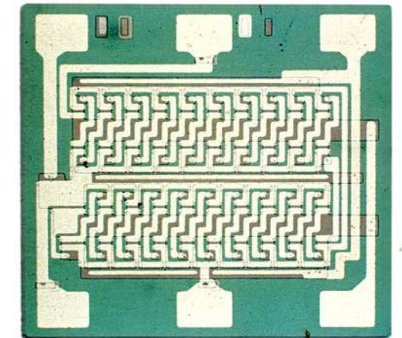
  > 1 milliard de transistors



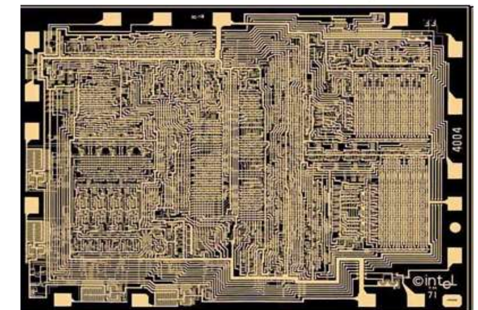
Fairchild FI 100
PMOS transistor



First commercial
MOS IC,
with **120 PMOS**



Intel i4004
with 2300 MOS



VLSI (Very Large Scale Intgegration)

FinFET by Intel

90 nm	65 nm	45 nm	32 nm	22 nm	14 nm	…
2003	2005	2007	2009	2011	2014	

13 metal layers

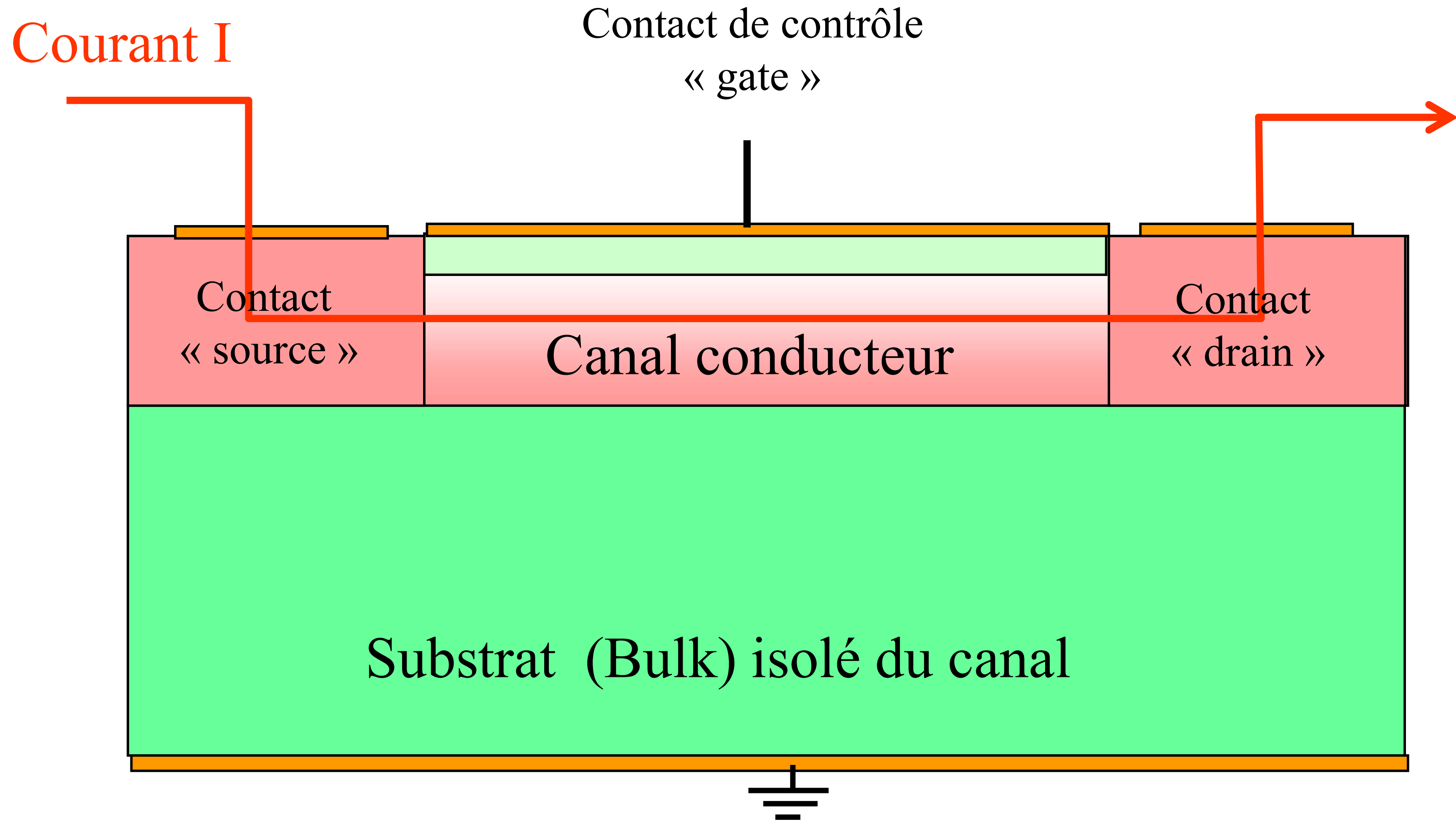
M. Bohr «Intel's Revolutionary 22 nm Transistor Technology», INTEL May 2011

http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf

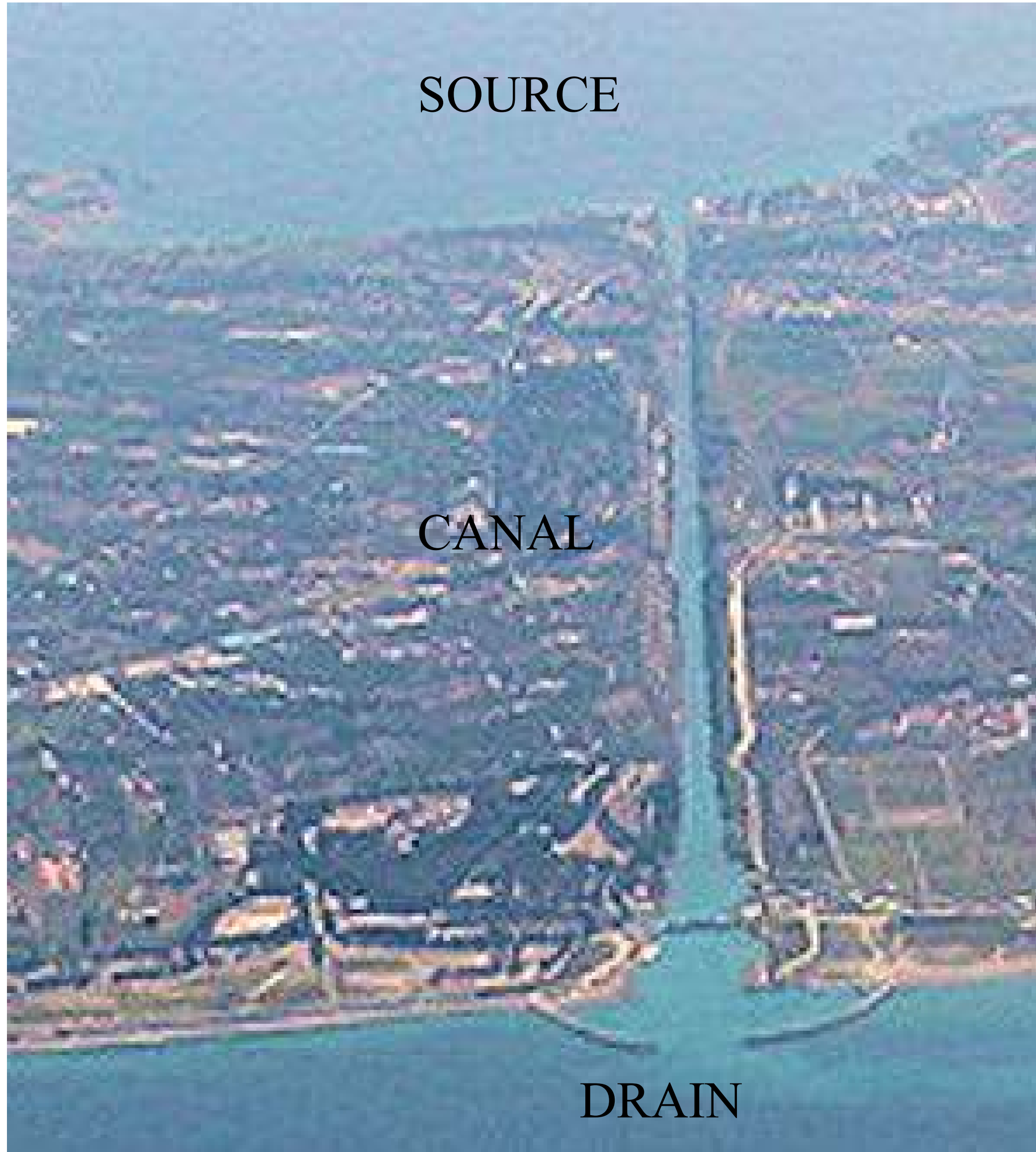
http://www.chipworks.com/en/technical-competitive-analysis/resources/blog/intels-14-nm-parts-are-finally-here/

PAB

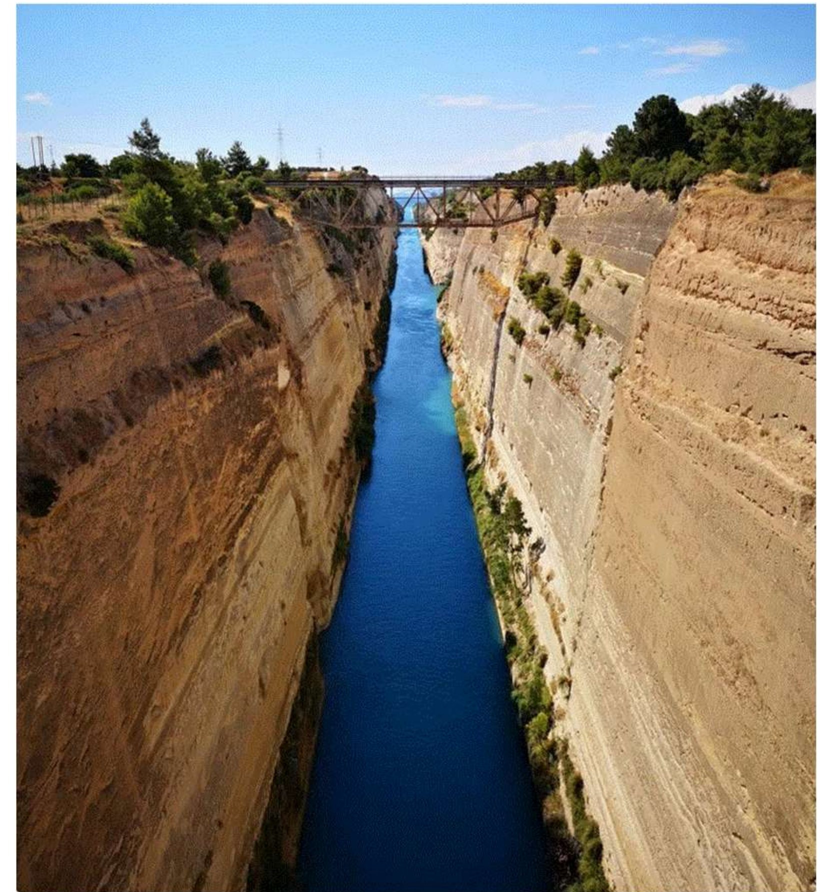
10.1: Principe du Field Effect Transistor (FET)



Analogie: FET

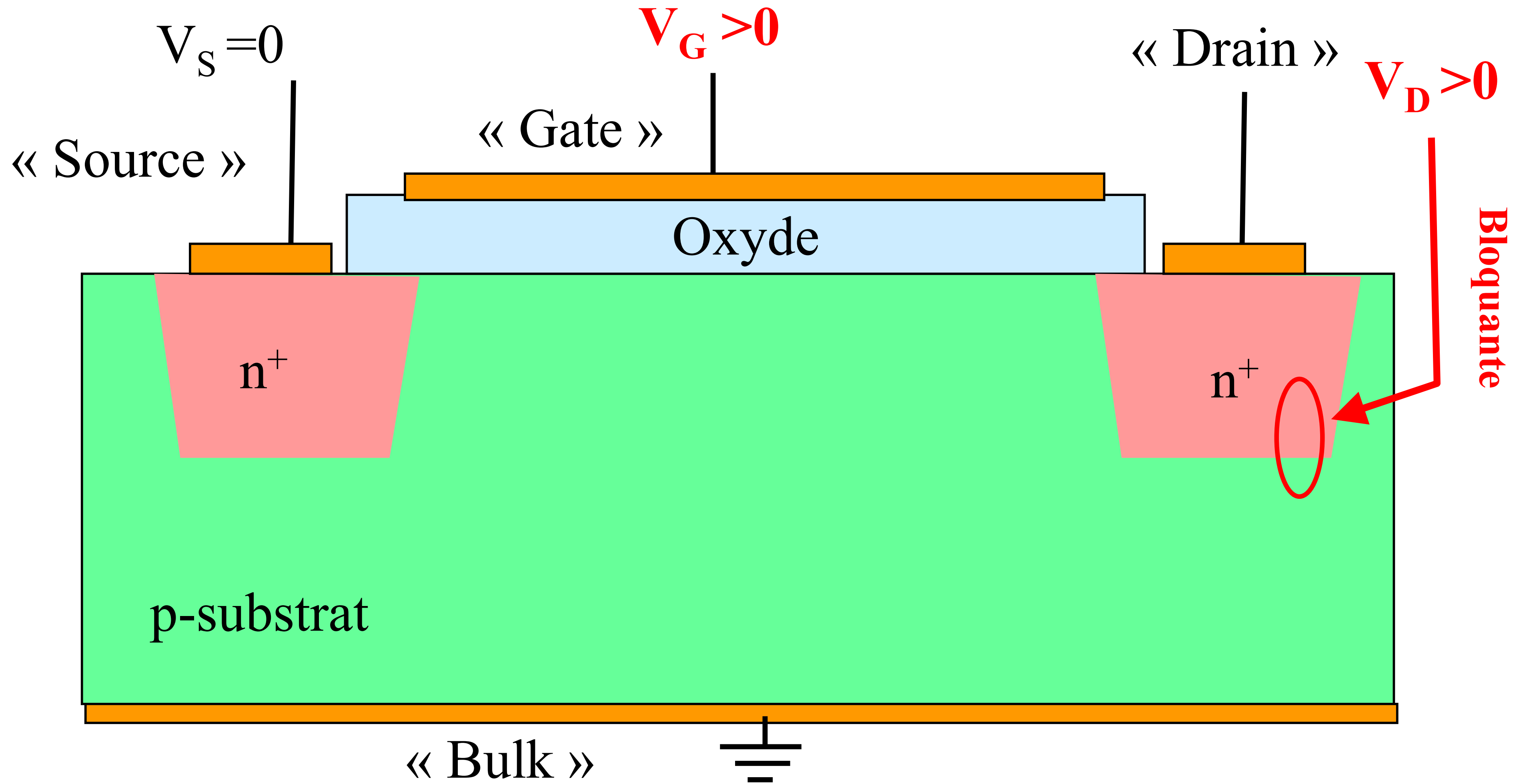


Canal de Corinthe



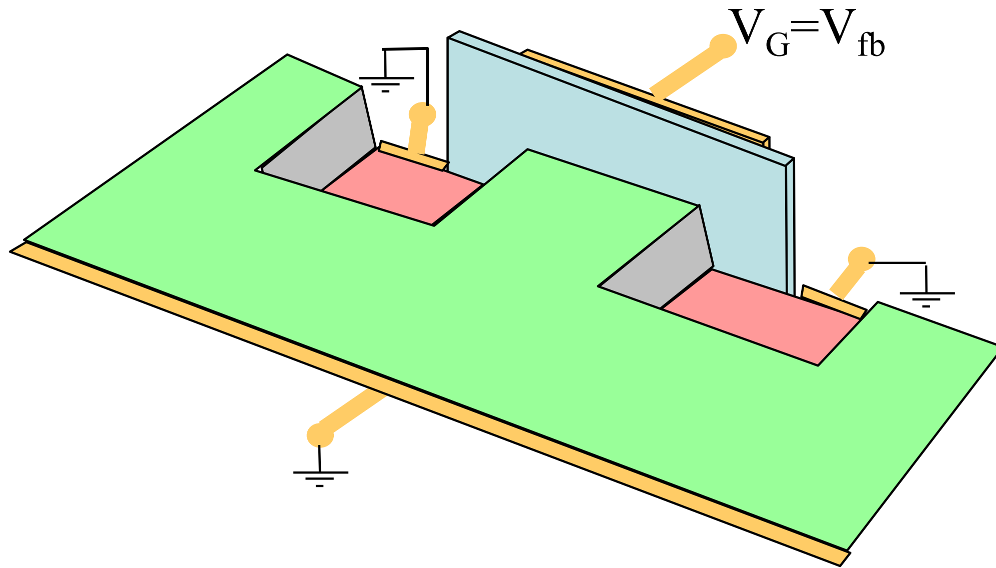
Exemple 1: le NMOS

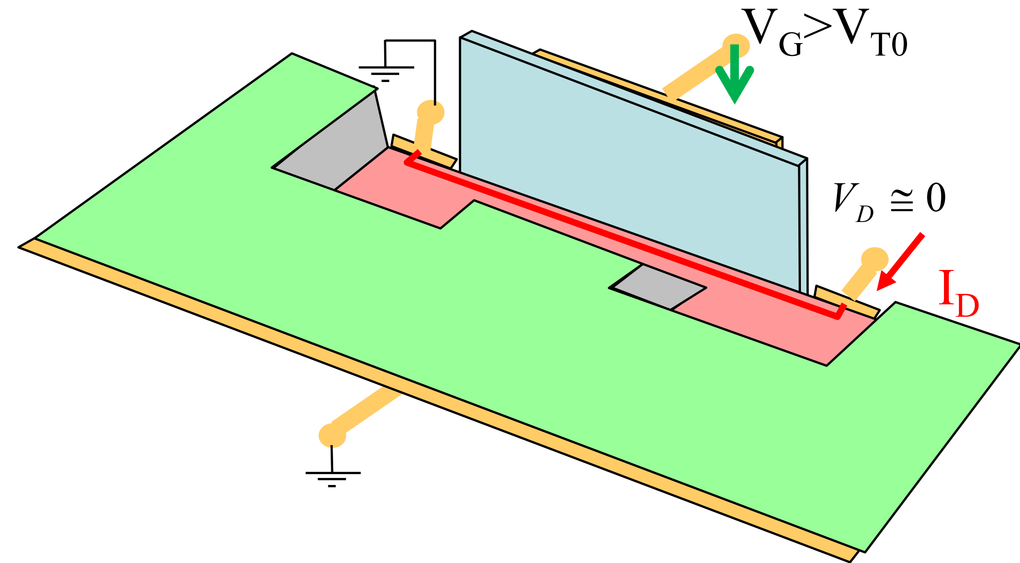
Attirer des électrons dans le canal



Le NMOS, un “enhancement” FET

Bande de conduction





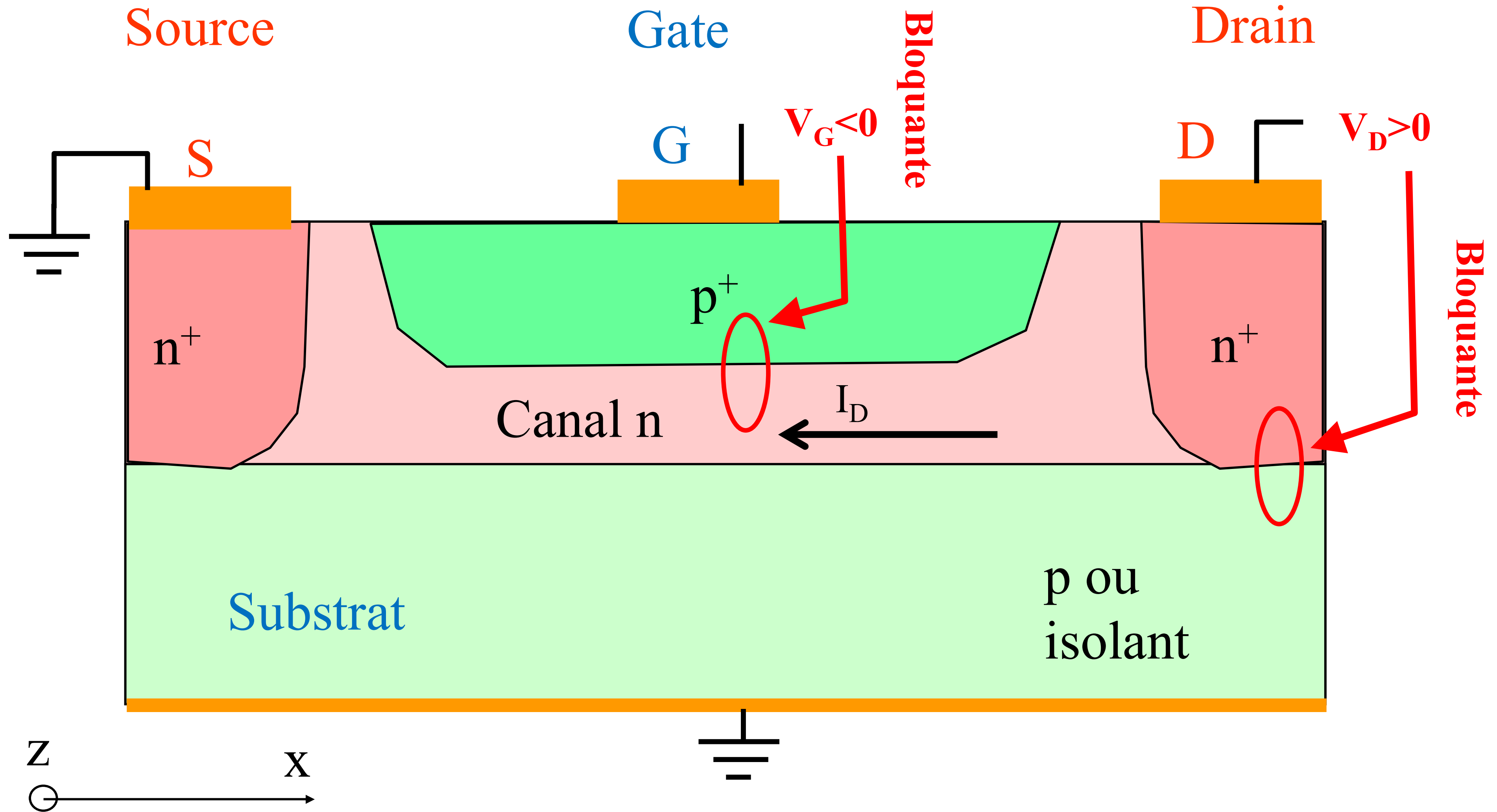
<u>Sans tension de gate</u>

<u>Avec tension de gate</u>

Le canal n’existe pas

Le canal est créé

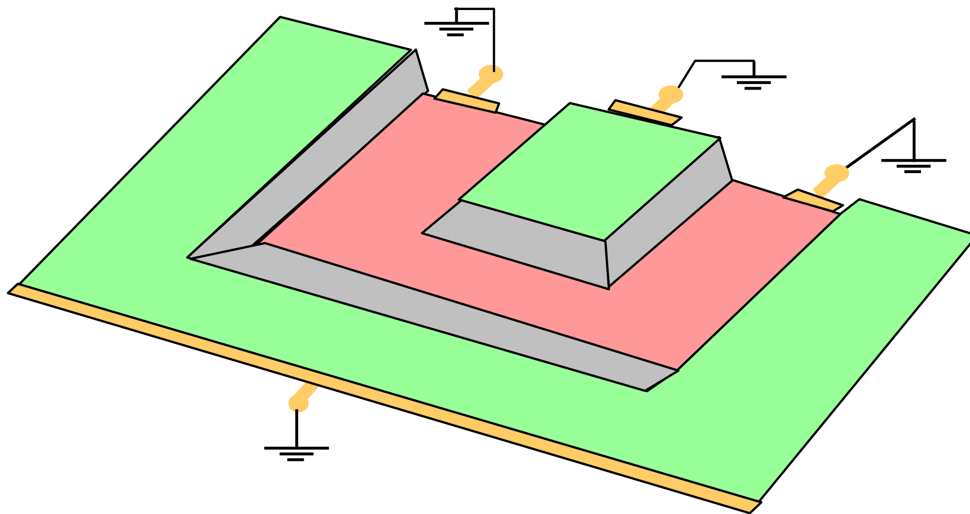
Exemple 2: le JFET à canal n

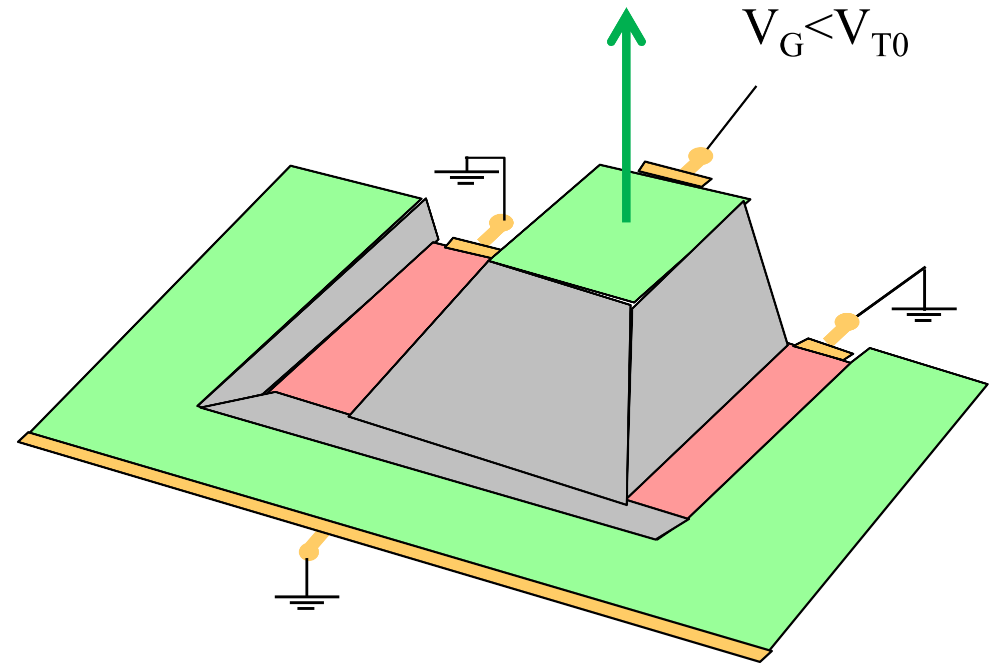


PAB

Le JFET à canal n: un « depletion » FET

Bande de conduction





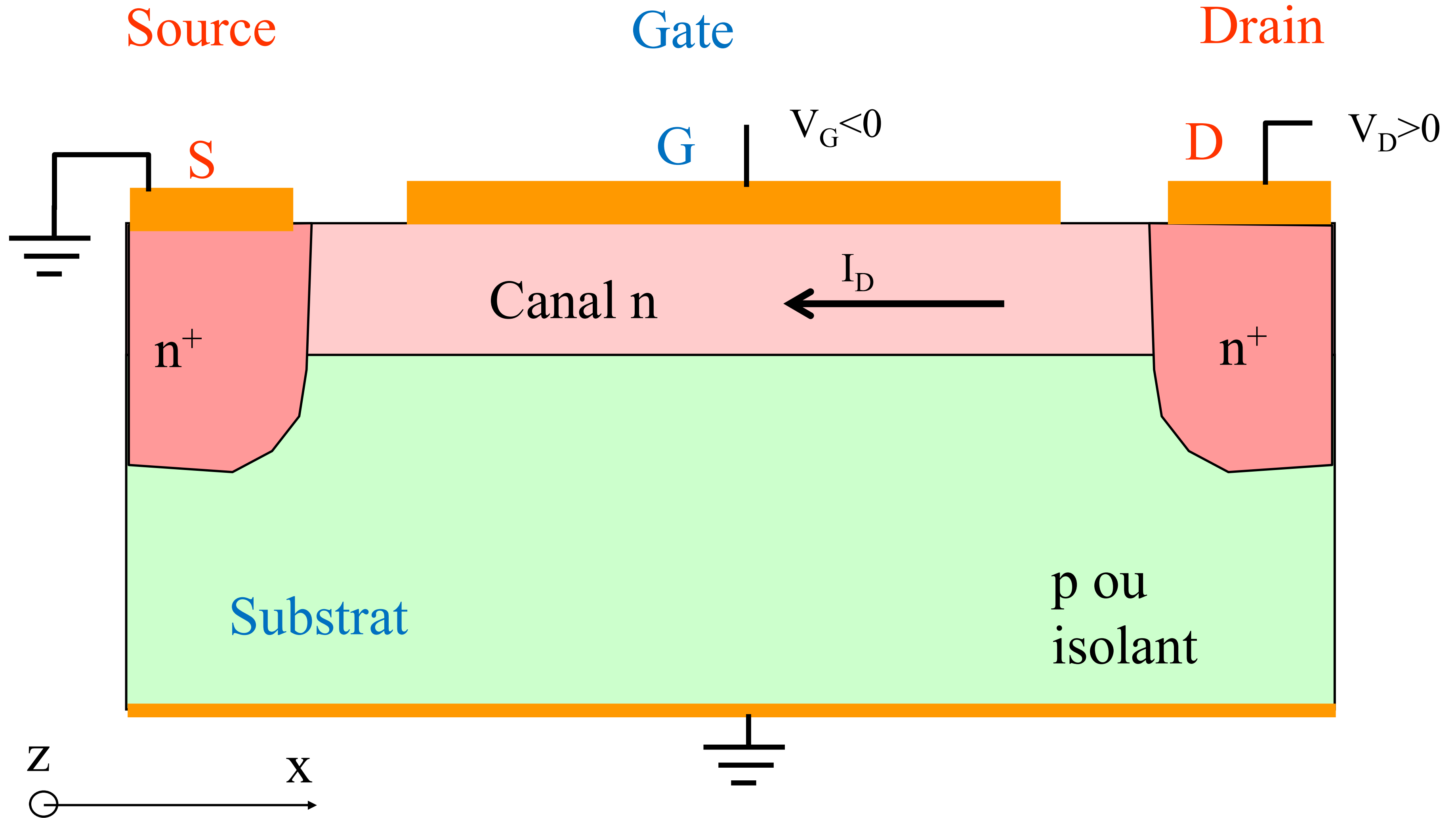
<u>Sans tension de gate</u>

<u>Avec tension de gate</u>

Le canal existe

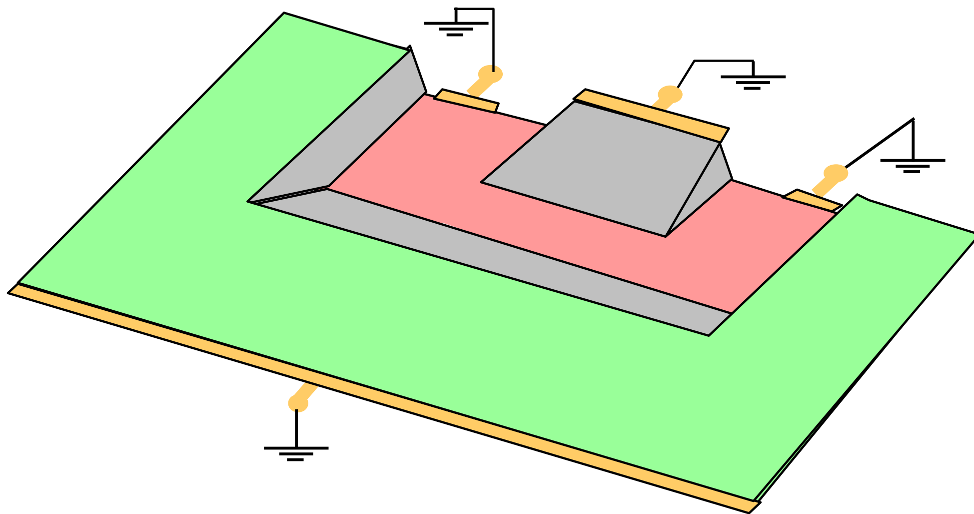
Le canal disparait

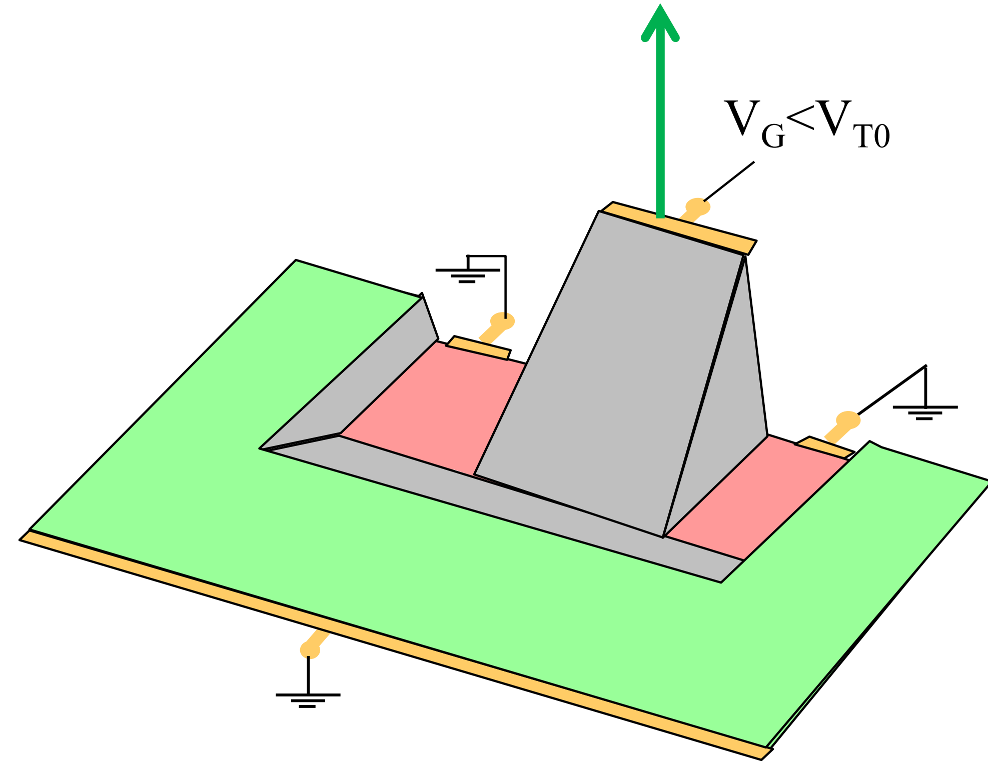
MESFET à canal n



MESFET à canal n

Bande de conduction





Sans tension de gate

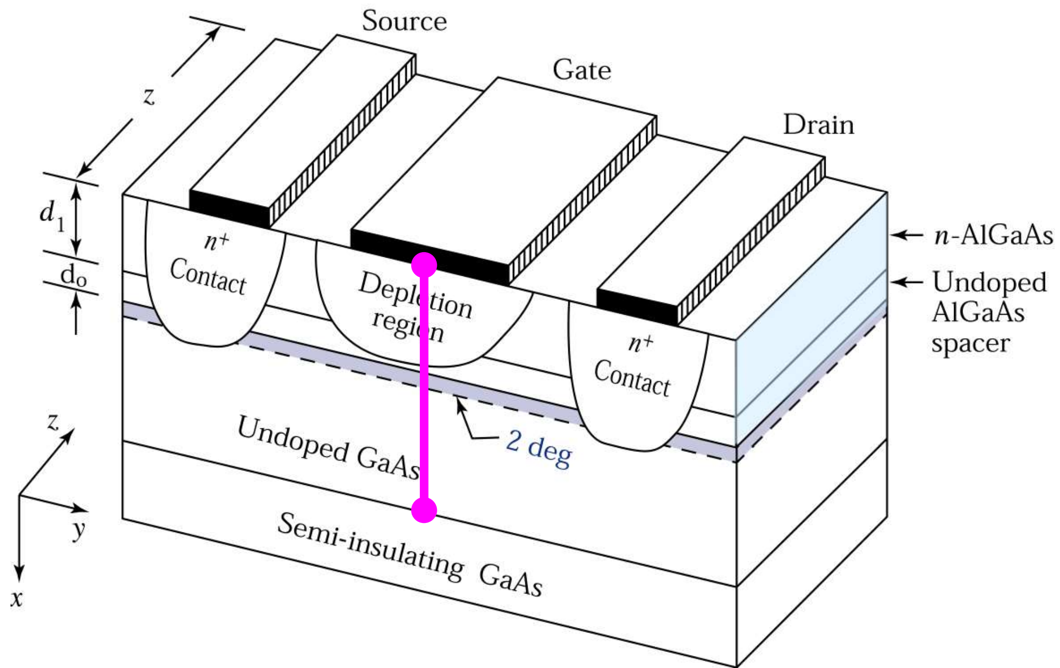
Avec tension de gate

Le canal existe

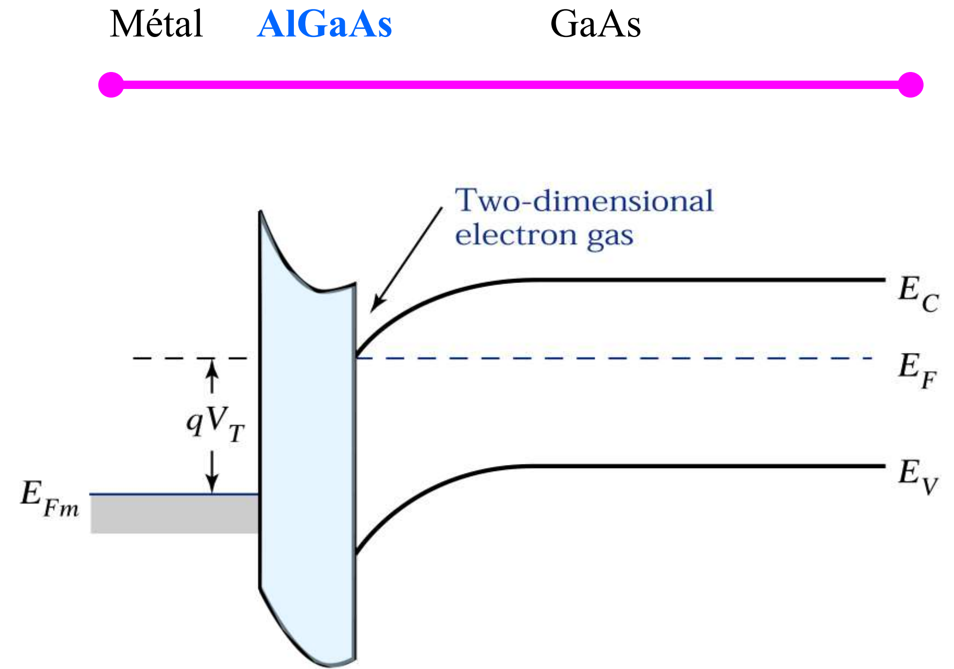
Le canal disparait

PAB

High Electron Mobility Transistors (HEMT)

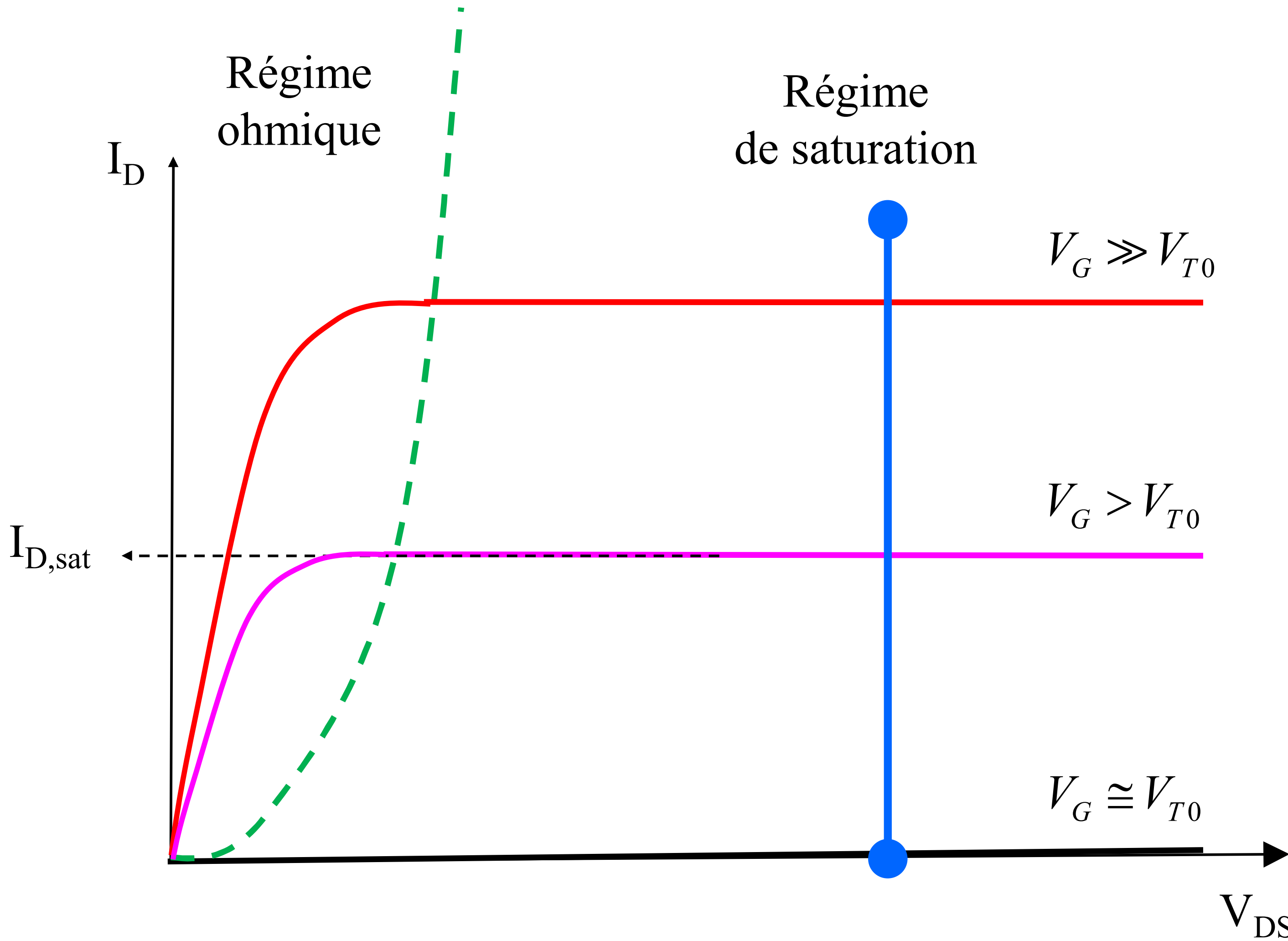


Semiconductor Devices, 2/E by S. M. Sze



Semiconductor Devices, 2/E by S. M. Sze

Courbes de sortie des FET idéaux (canal n)

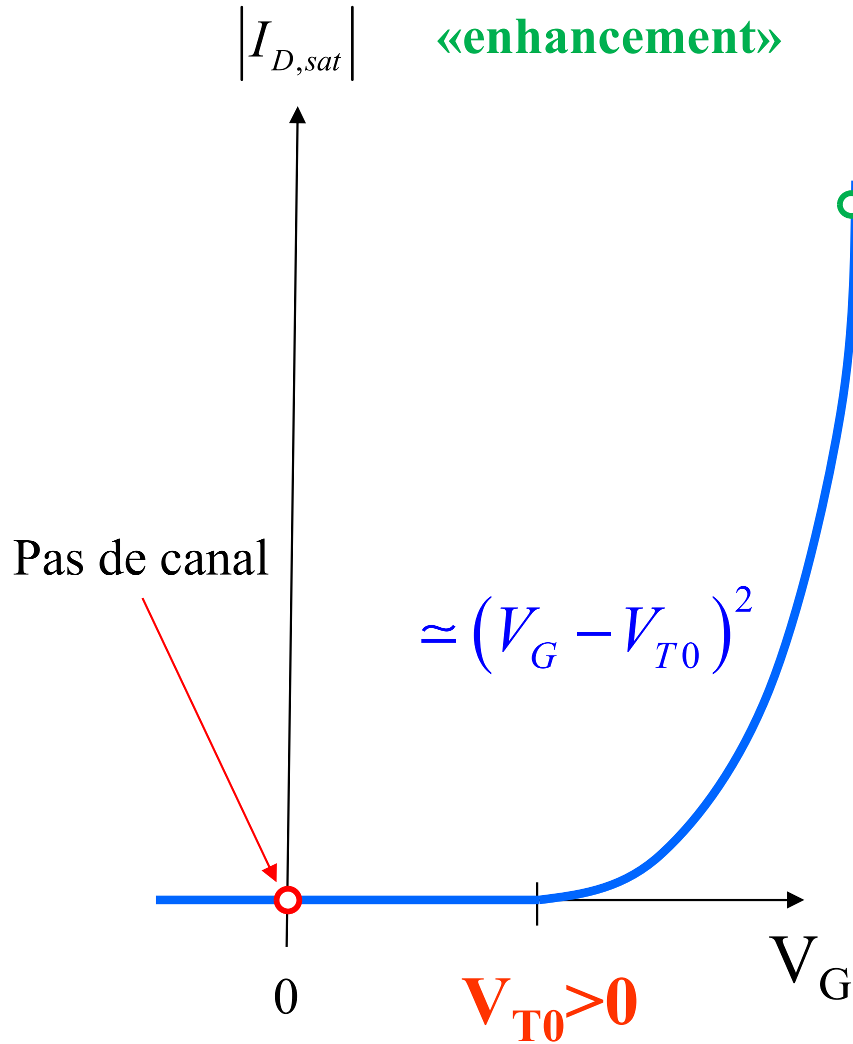


NMOS	N-JFET
$V_G \gg 0$	$V_G = 0$
$V_G > 0$	$V_G < 0$
$V_G = 0$	$V_G << 0$
$V_{T0} > 0$	$V_{T0} < 0$

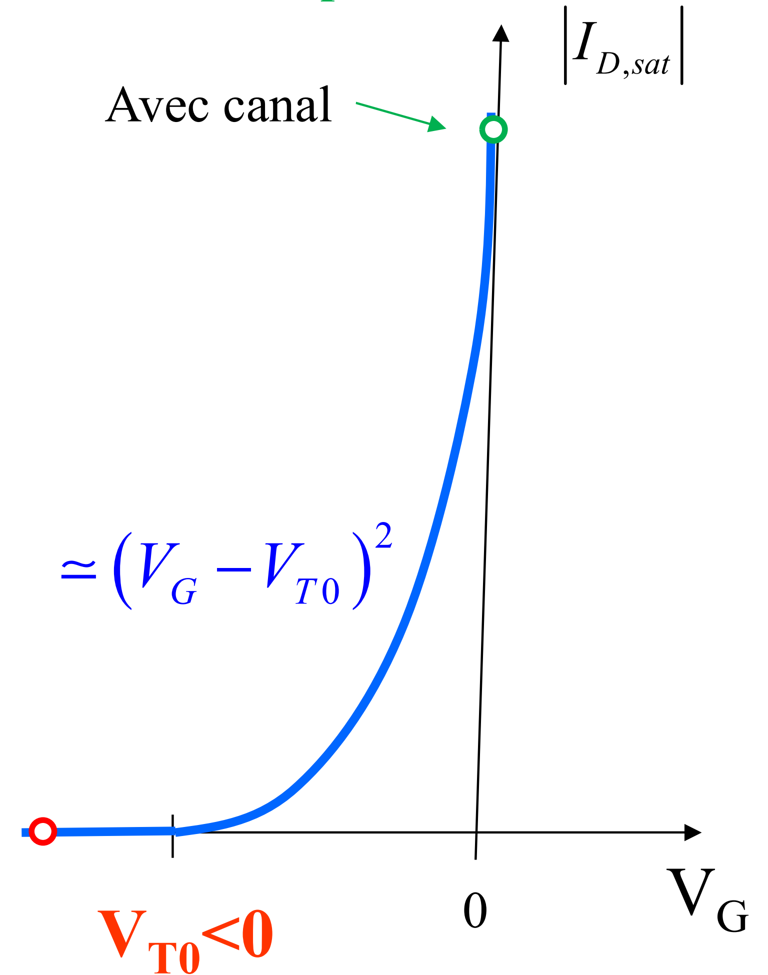
PAB

Tension de threshold et courbe $I_{D,sat}(V_G)$

NMOS «enhancement»

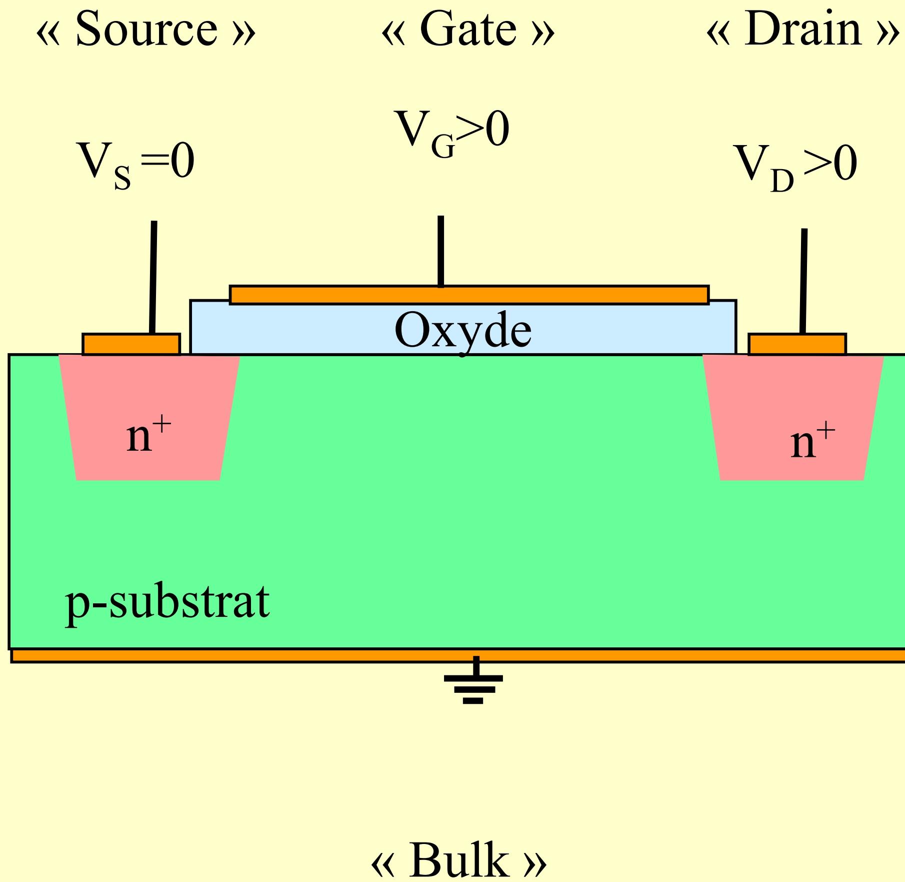


JFET à canal N «depletion»

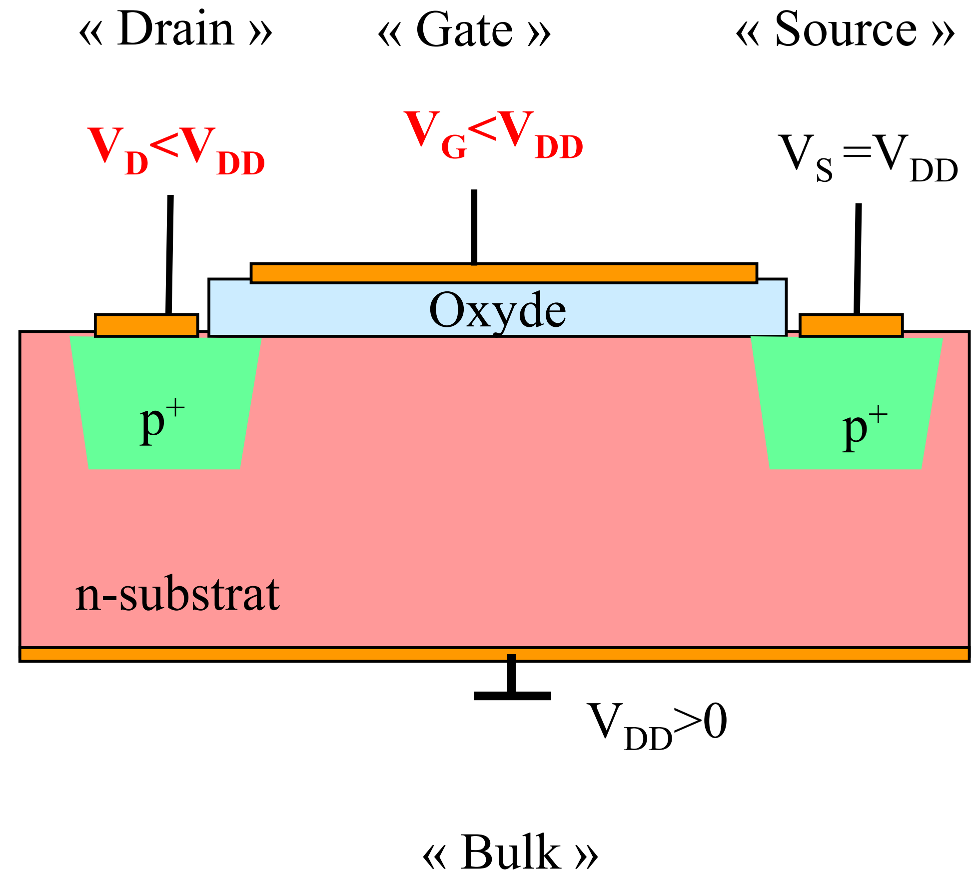


10.2: Structure MOSFET

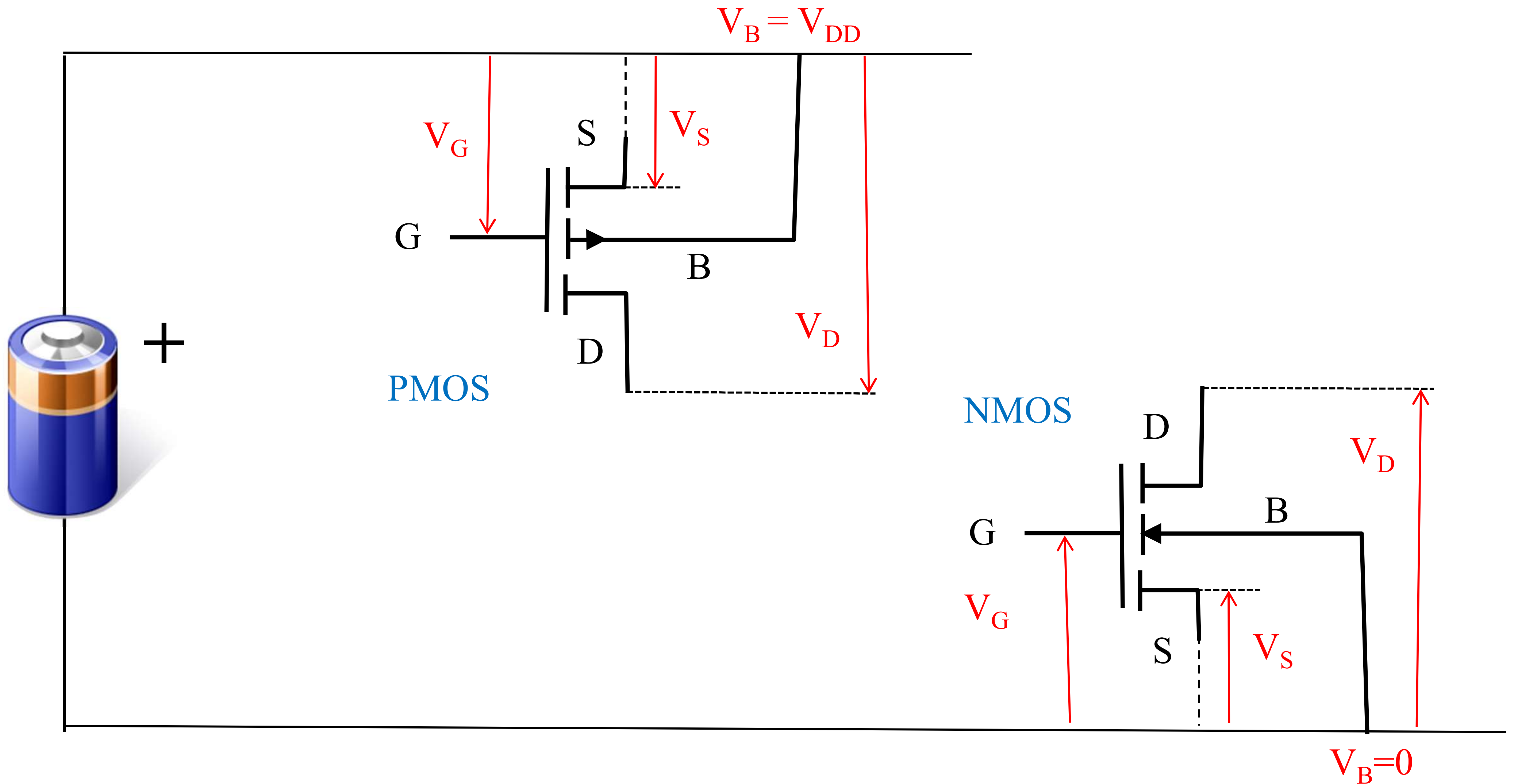
NMOS: MOSFET à canal n



PMOS: MOSFET à canal p



MOSFET: définition des tensions



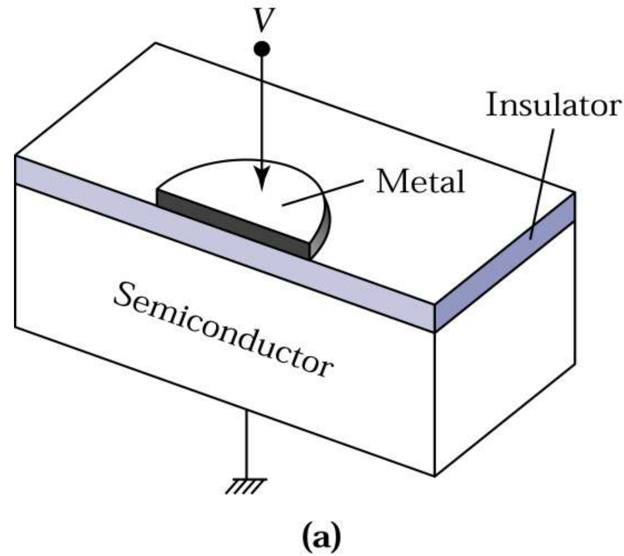
NMOS

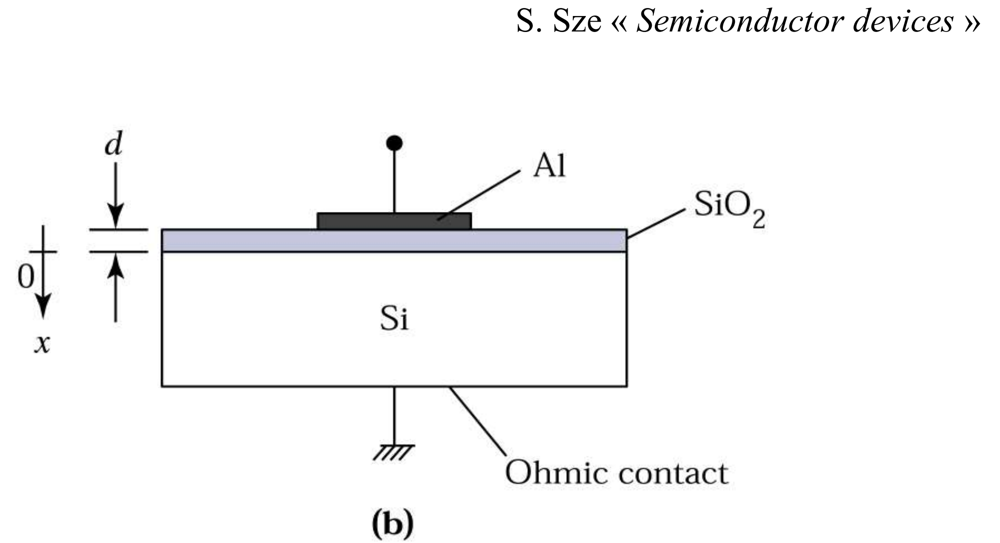
Source
Gate
Drain
SiO_2
Z
L
d
n^+
r_j
n^+
p
Substrate

2/E by S. M. Sze

Rappel: structure MOS

S. Sze « *Semiconductor devices* »





"Metal"

Al, Au,
(electromigration)

Poly-Si, Silicide

Oxide

SiO_2, High k (HfSiON)

$d_{ox} \cong 10\, nm$

$C_{ox} = \varepsilon_r \varepsilon_0 \frac{A}{d_{ox}}$

$\varepsilon_r \cong 4 \quad (SiO_2)$

Semiconductor

Silicon

$N \approx 10^{16}\, cm^{-3} \rightarrow 10^{18}\, cm^{-3}$

Résumé: Formules avec slope factor n

$\psi_s \cong 0$ $Q_n \cong 0$ $\psi_s \cong 2\psi_B$

Flat Band

Inversion faible

Inversion forte

ψ_B $2\psi_B$ ψ_s

0

$$\frac{V_G - V_{M0}}{n} \cong \psi_s - 2\psi_B$$

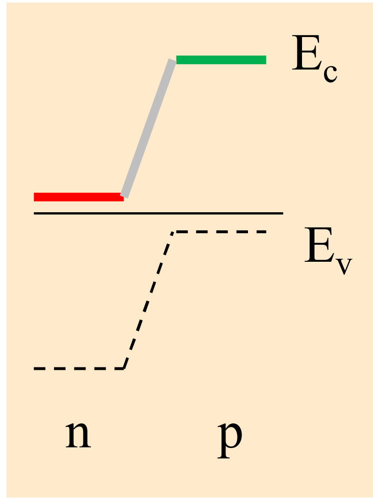
$$Q_n \cong -C_{ox}(V_G - V_{M0})$$

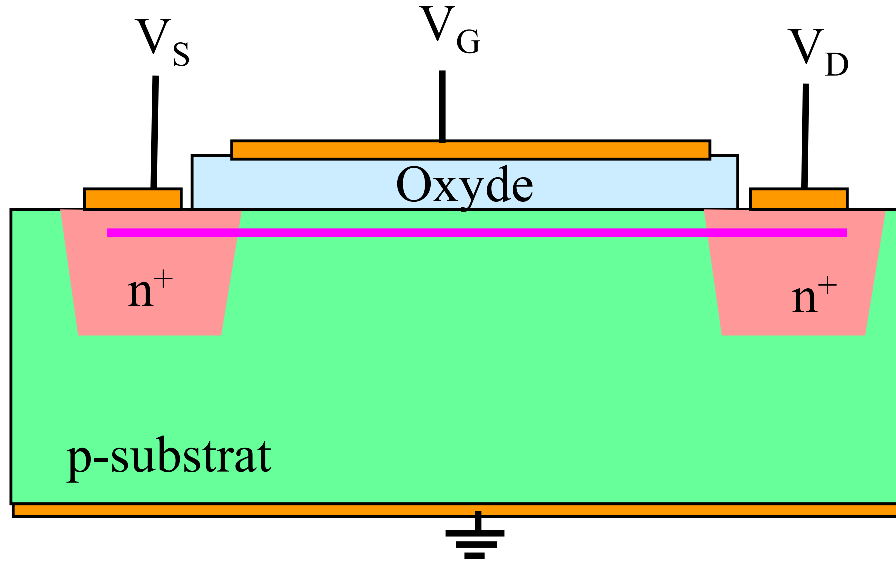
V_G

$$V_{fb} = \phi_m - \phi_s$$

$$V_{M0} - V_{fb} = (2n-1)\cdot 2\psi_B$$

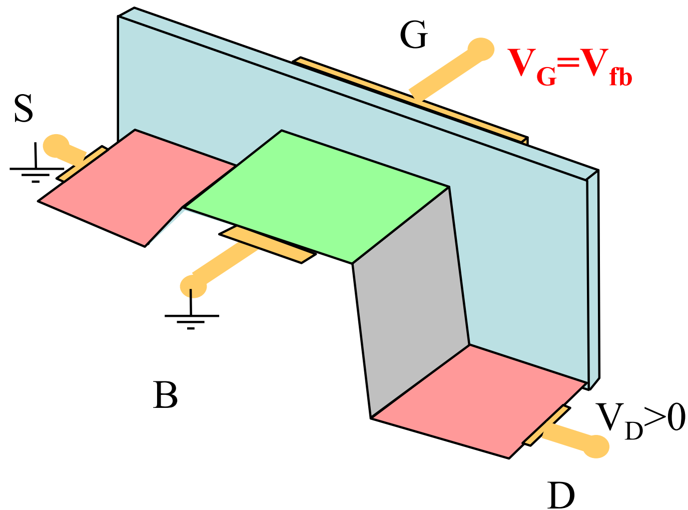
10.3: Fonctionnement « sub-threshold »



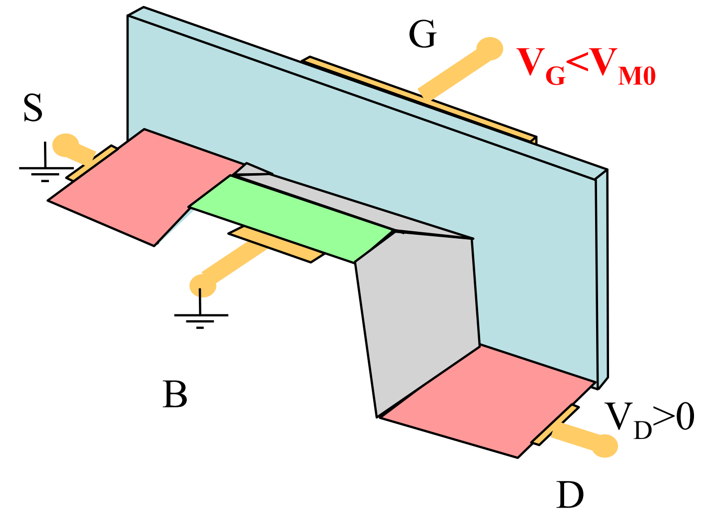


→ **Structure npn**

Flat-band

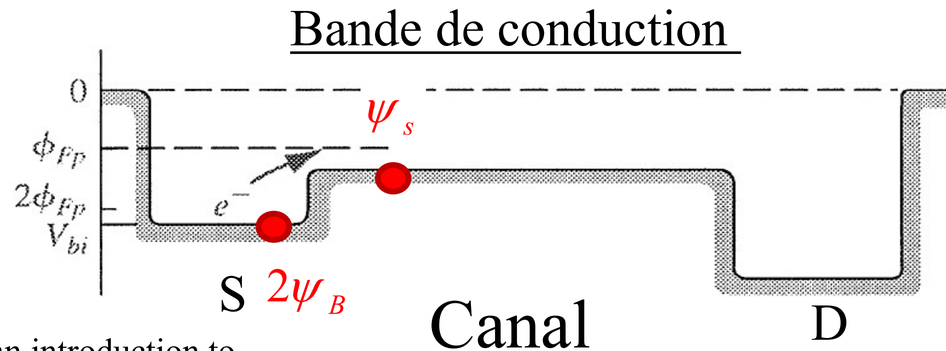


Inversion faible

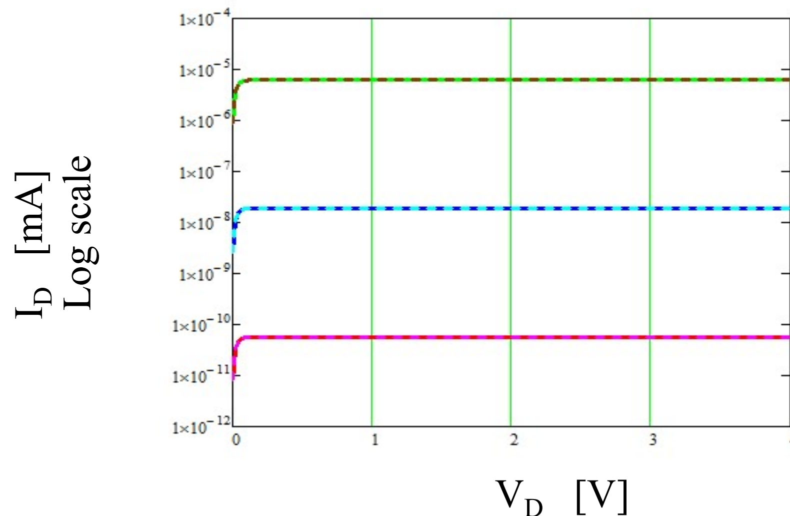


Fonctionnement « sub-threshold »: inversion faible

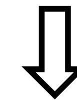
- Comportement similaire à un transistor bipolaire npn
- Pas de champ électrique → courant de diffusion



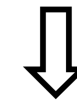
Neamen, « an introduction to semiconductor devices »



$$\frac{V_G - V_{M0}}{n} \cong (\psi_s - 2\psi_B) - \frac{Q_n}{nC_{ox}}$$



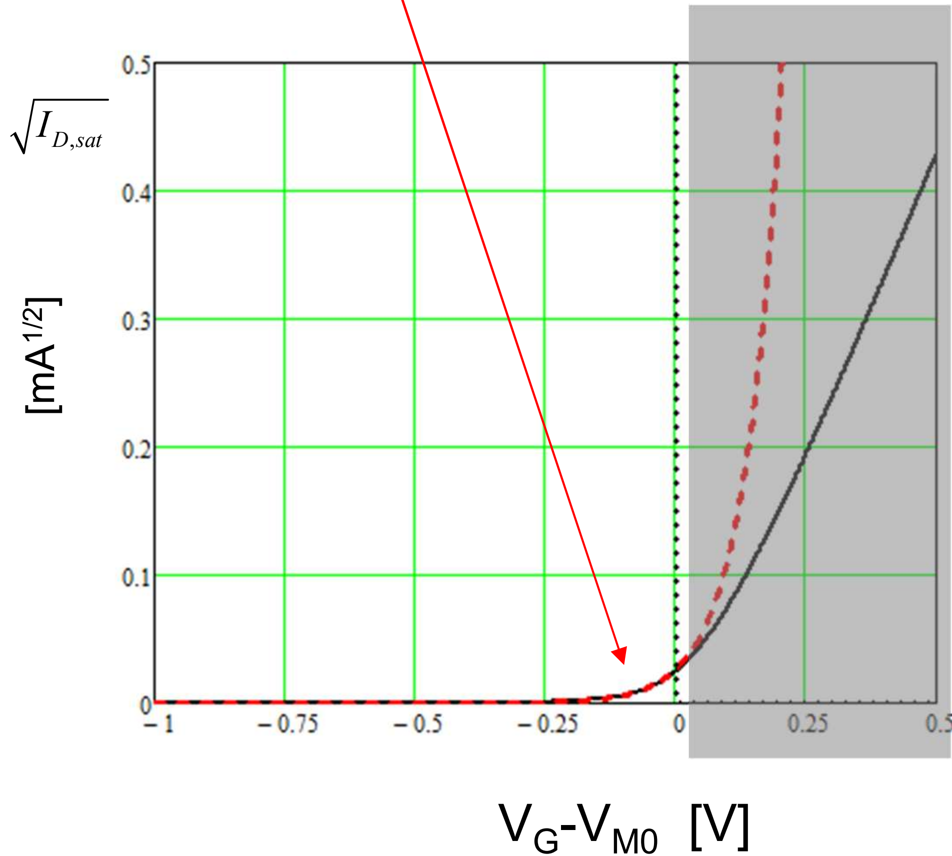
$$I_{D,sat} \approx I_{sub,0} \cdot e^{\frac{(V_G - V_{M0})}{n} \cdot \frac{1}{U_T}}$$

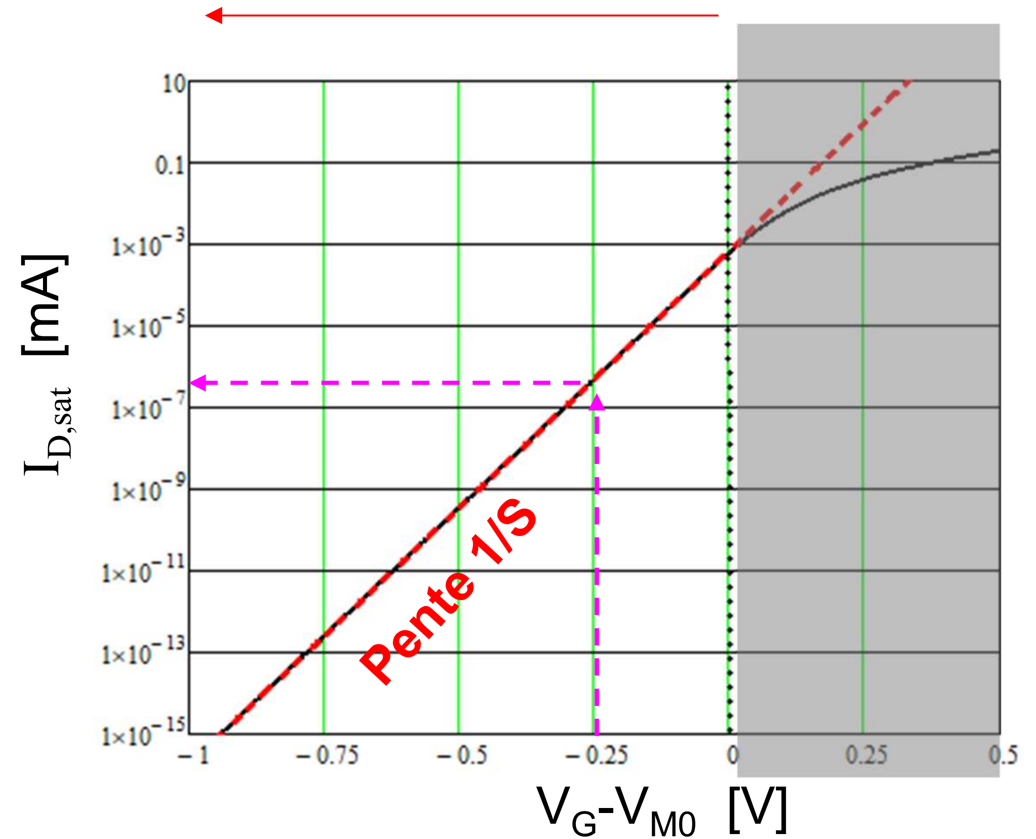


$$\frac{g_{m,sat}}{I_{D,sat}} \equiv \frac{1}{I_{D,sat}} \cdot \frac{\partial I_{D,sat}}{\partial V_G} \approx \frac{1}{n \cdot U_T}$$

Opération « sub-threshold »: exemple en mode actif ($V_D > V_{D,sat}$)

PAB





C_{ox}=3fF/um^2
W/L=10
T=300 K

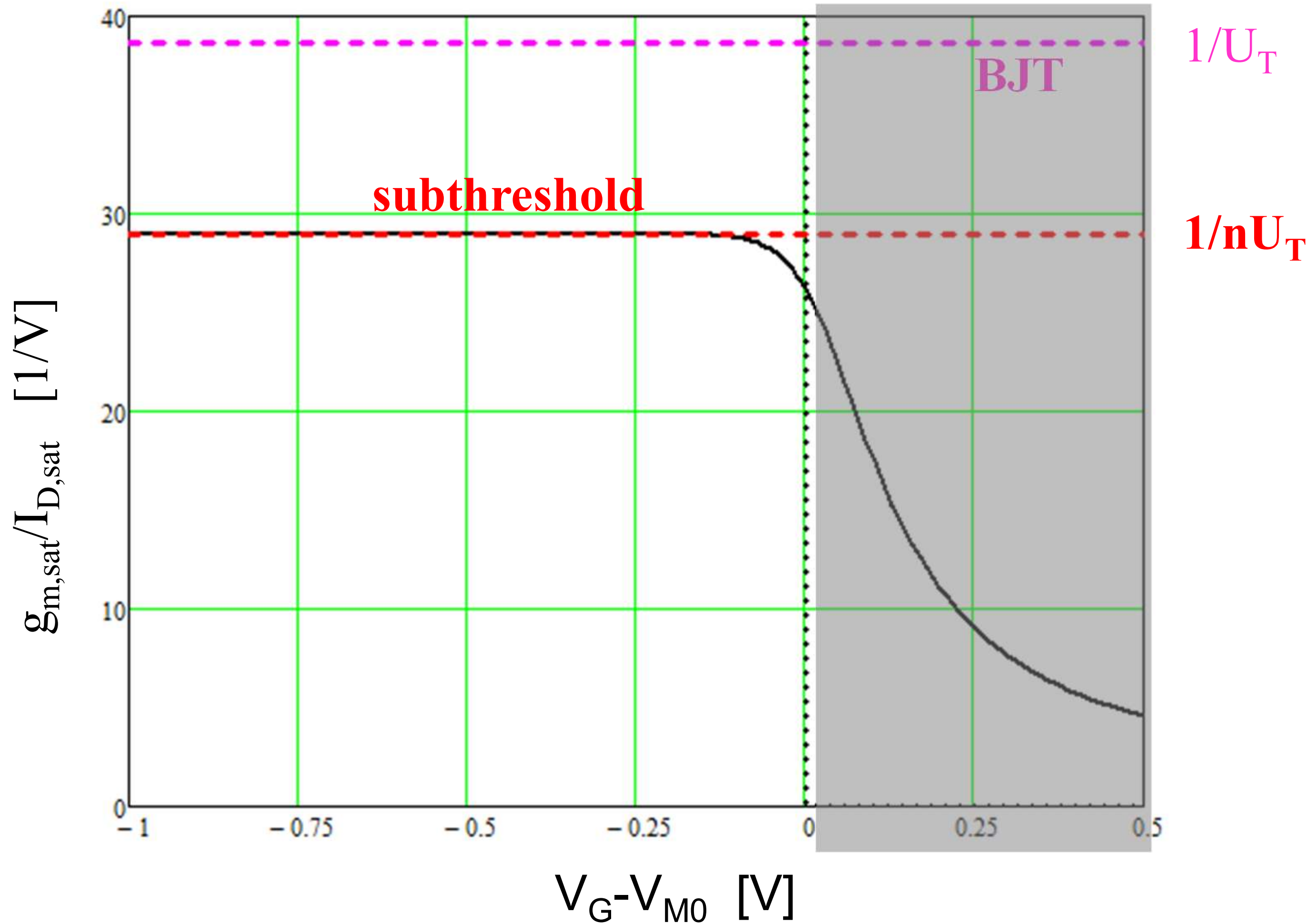
u_n=1000cm^2/V.s
n=4/3

$$S = n \cdot U_T \cdot Ln(10)$$

300K → S=n.60 mV/dec.

PAB

Transconductance en saturation: g_m/I_D



Transconductance définition

$$g_{m,sat} \equiv \frac{\partial I_{D,sat}}{\partial V_G}$$

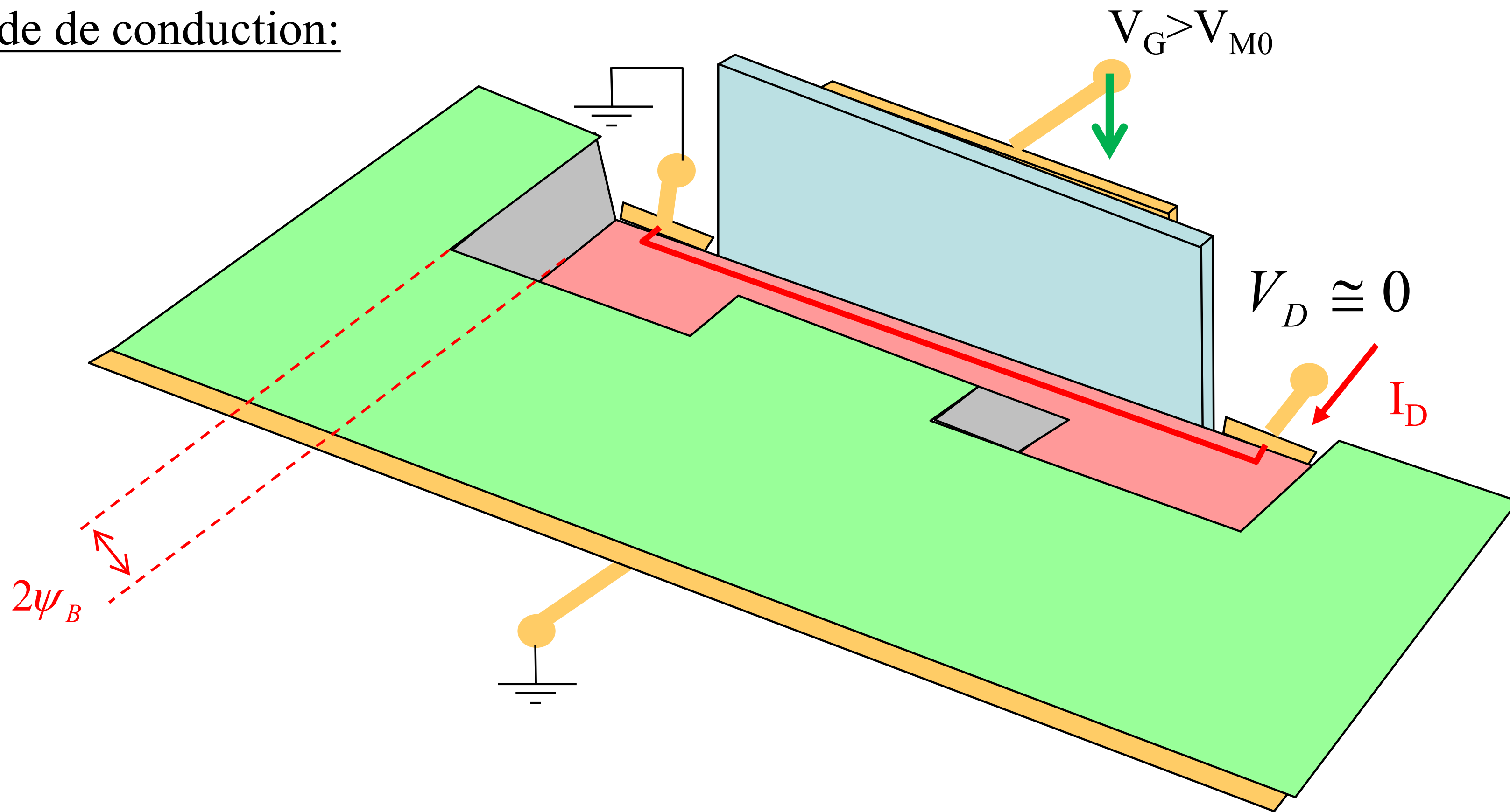
C_{ox}=3fF/um^2
W/L=10
T=300 K

u_n=1000cm^2/V.s
n=4/3

PAB

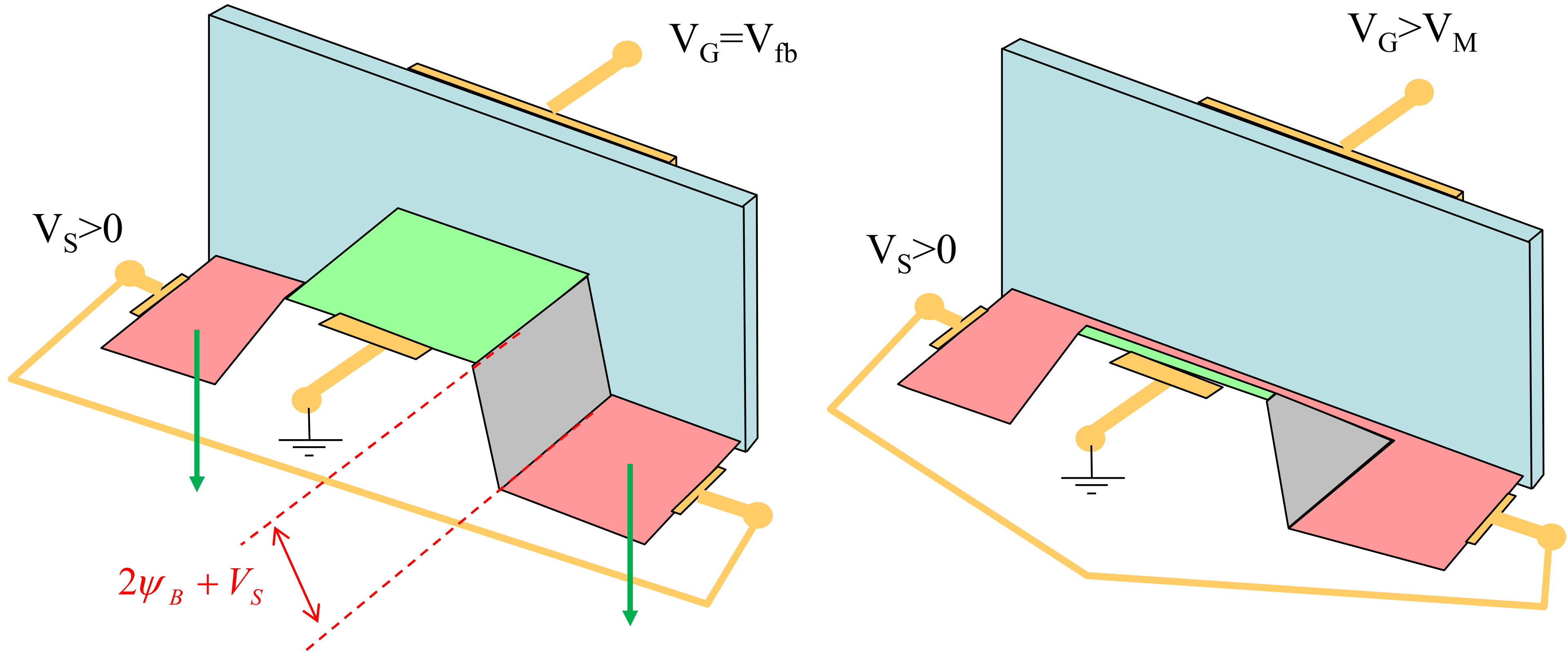
10.4: NMOS en inversion forte, régime linéaire

Bande de conduction:



$$|Q_n| = C_{ox} (V_G - V_{M0})$$

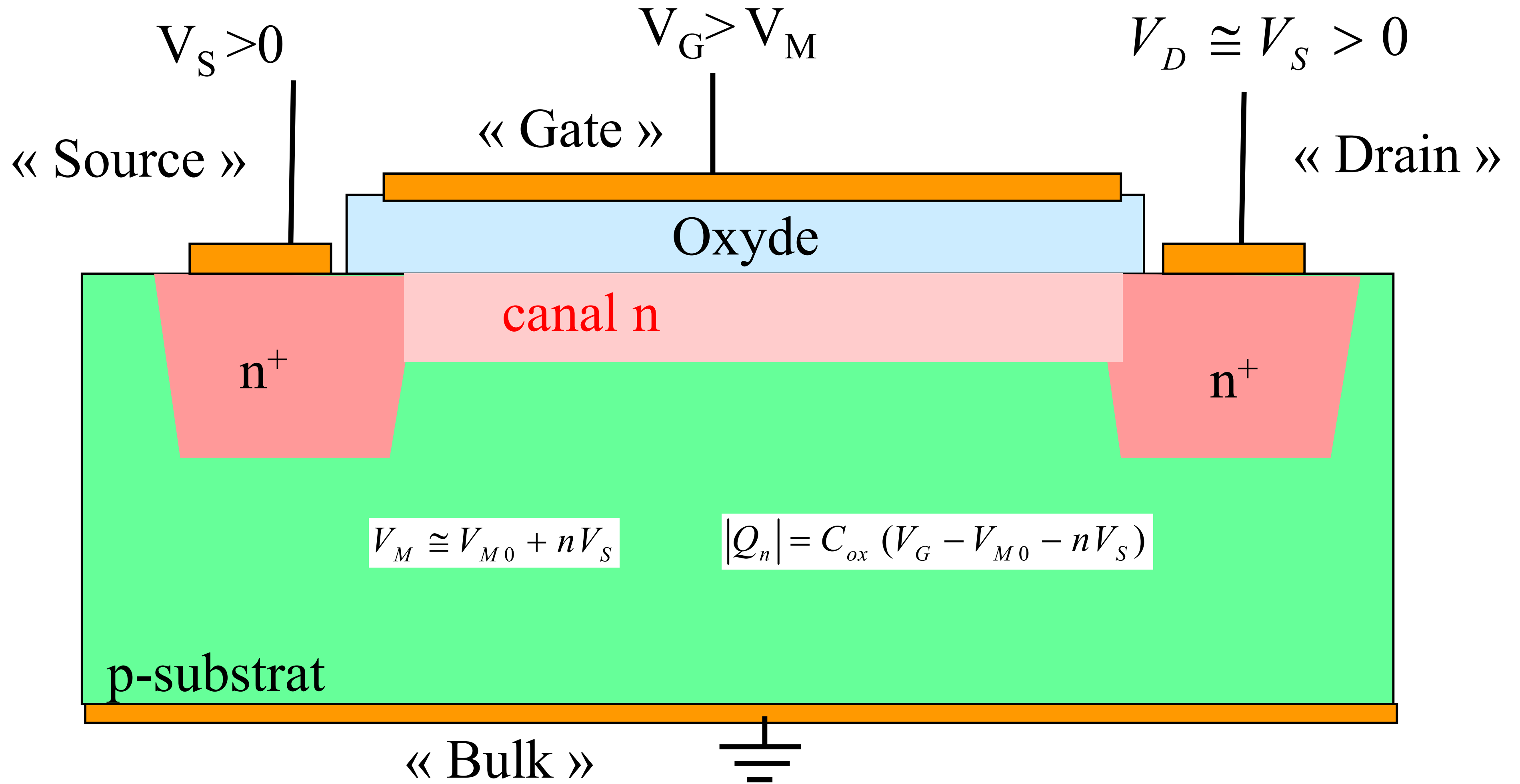
Influence de V_S



Threshold: $V_G - V_{M0} \cong n \cdot (\psi_s - 2\psi_B) \quad \Rightarrow \quad V_M - V_{M0} \cong n \cdot V_S$

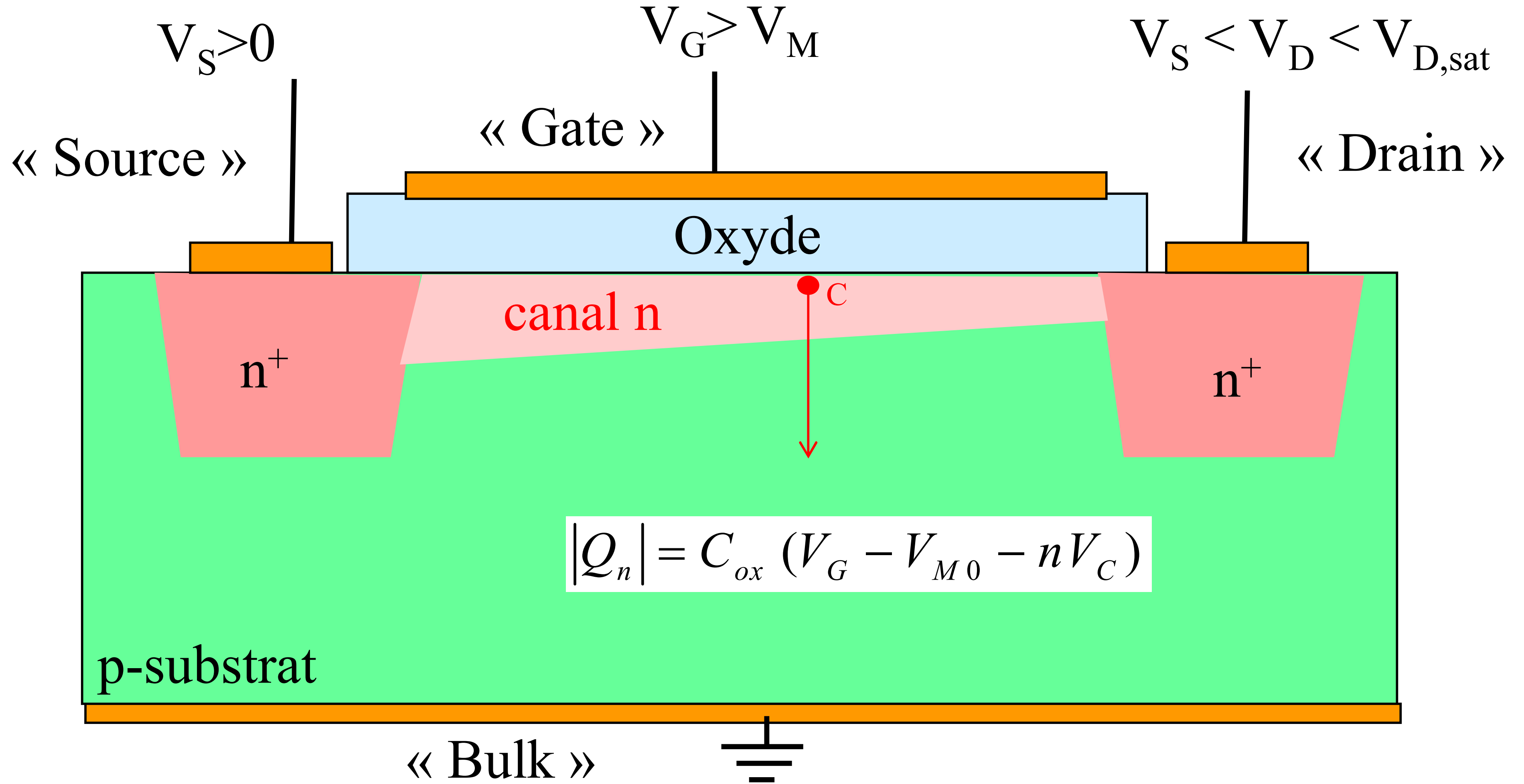
Inversion: $V_G > V_M$ $\quad Q_n = -C_{ox}(V_G - V_{M0} - nV_S)$

Influence de V_S



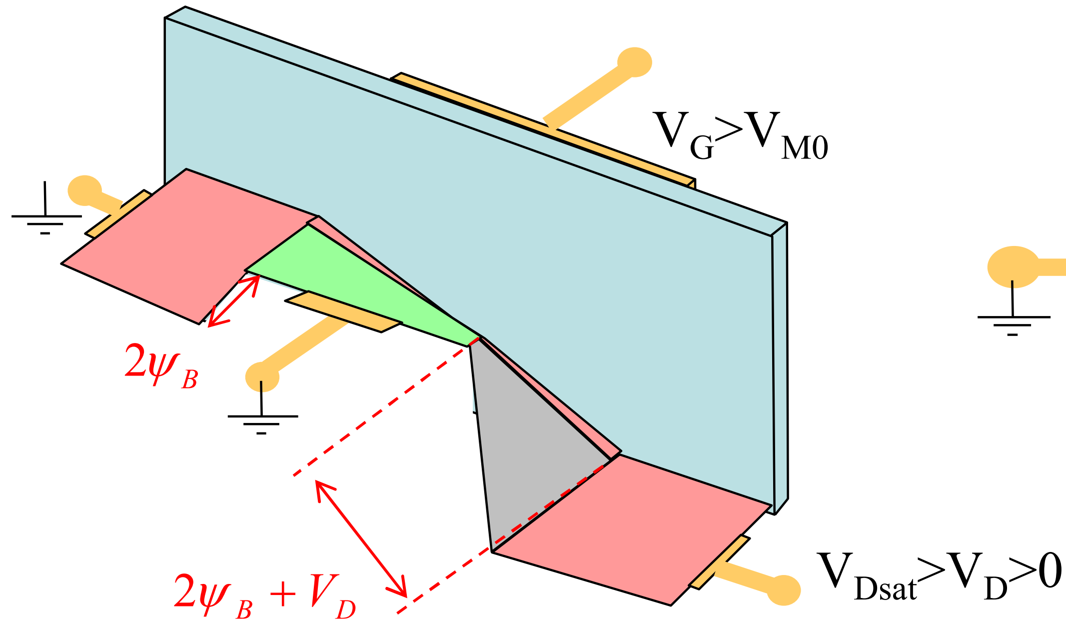
PAB

NMOS en inversion forte, régime ohmique

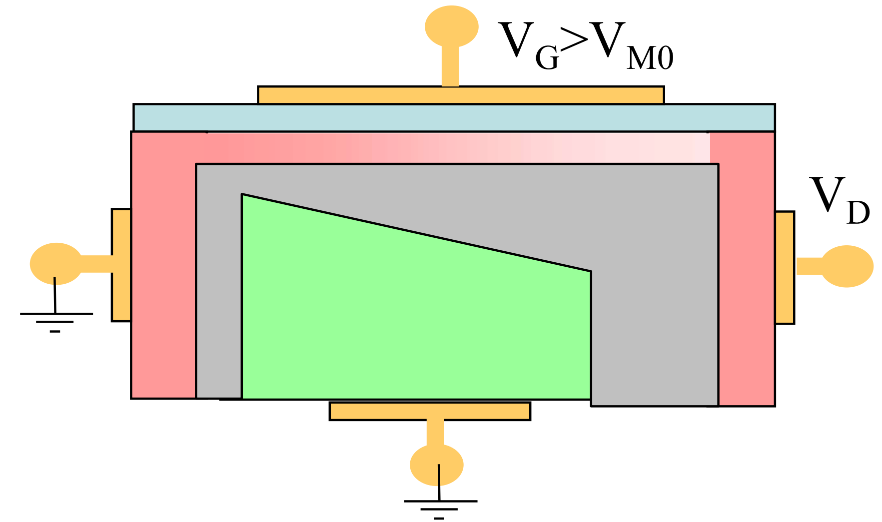


Régime FET ohmique: vision 3D

Bande de conduction:

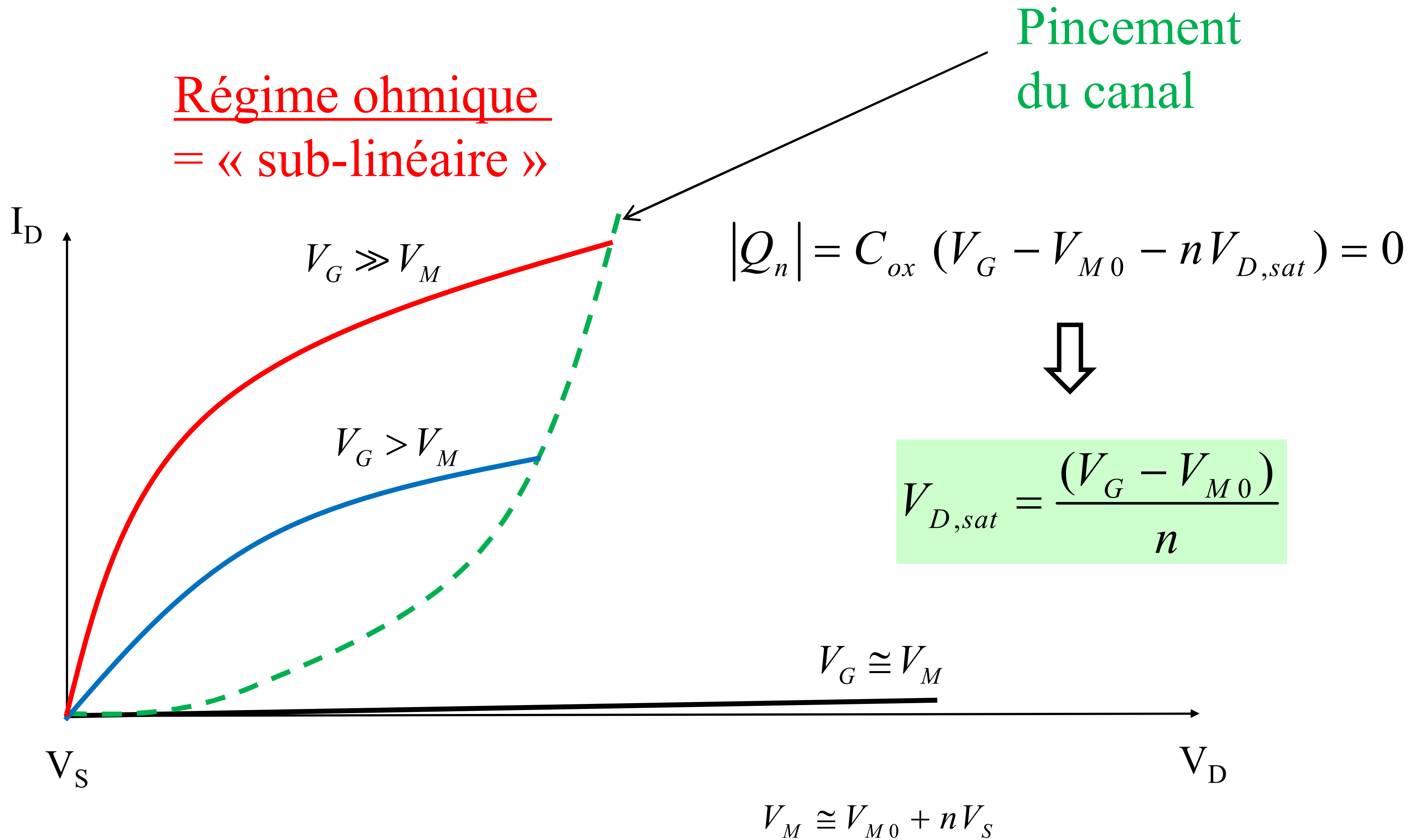


Vue latérale:



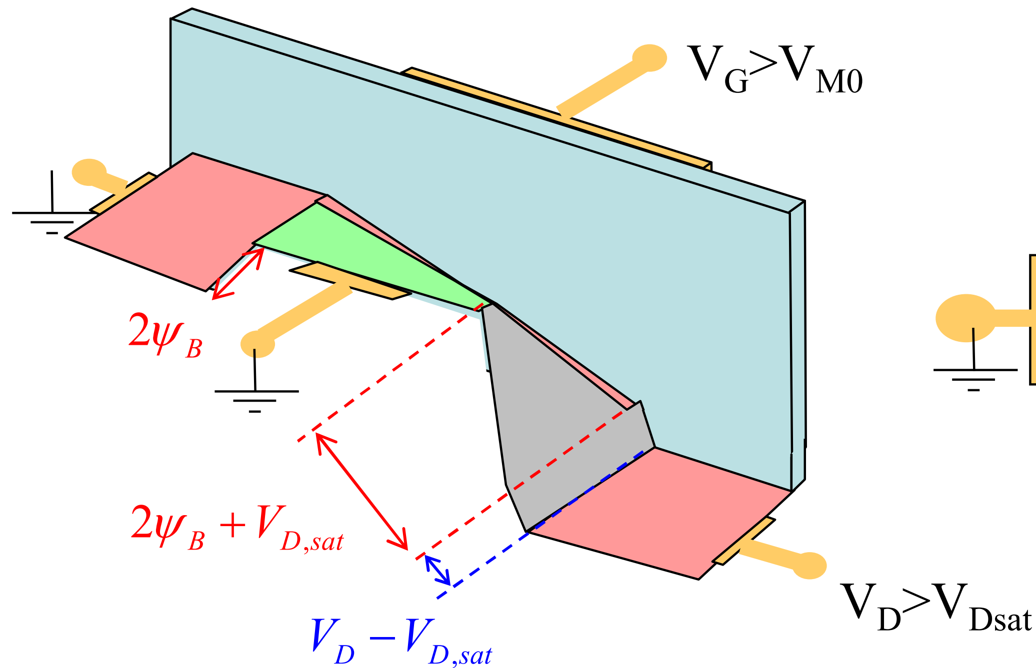
Les charges dans le canal diminuent lorsqu'on s'approche du drain

Régime FET ohmique: courbes caractéristiques

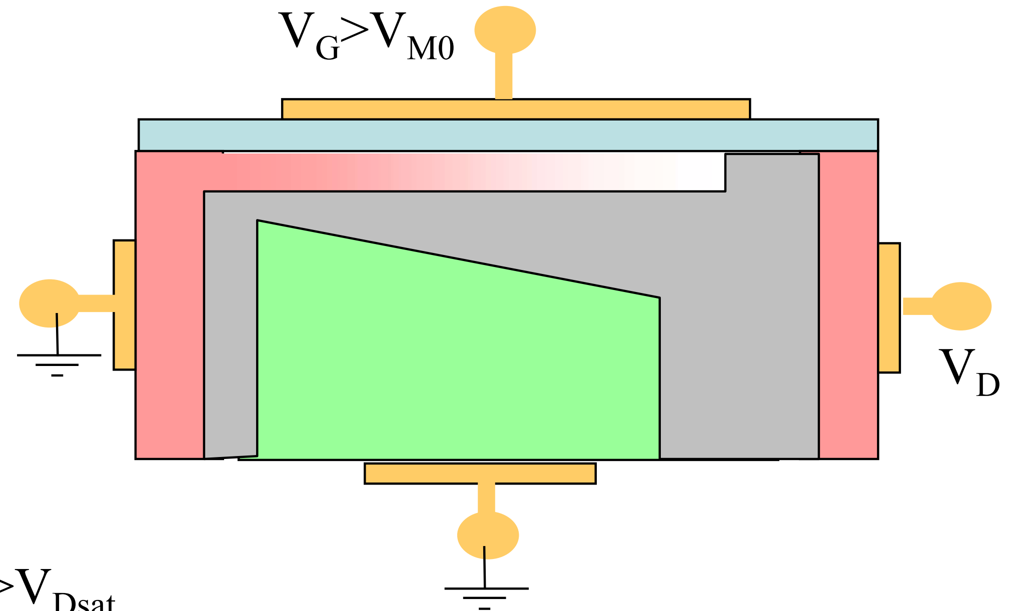


Pincement du canal: vision 3D

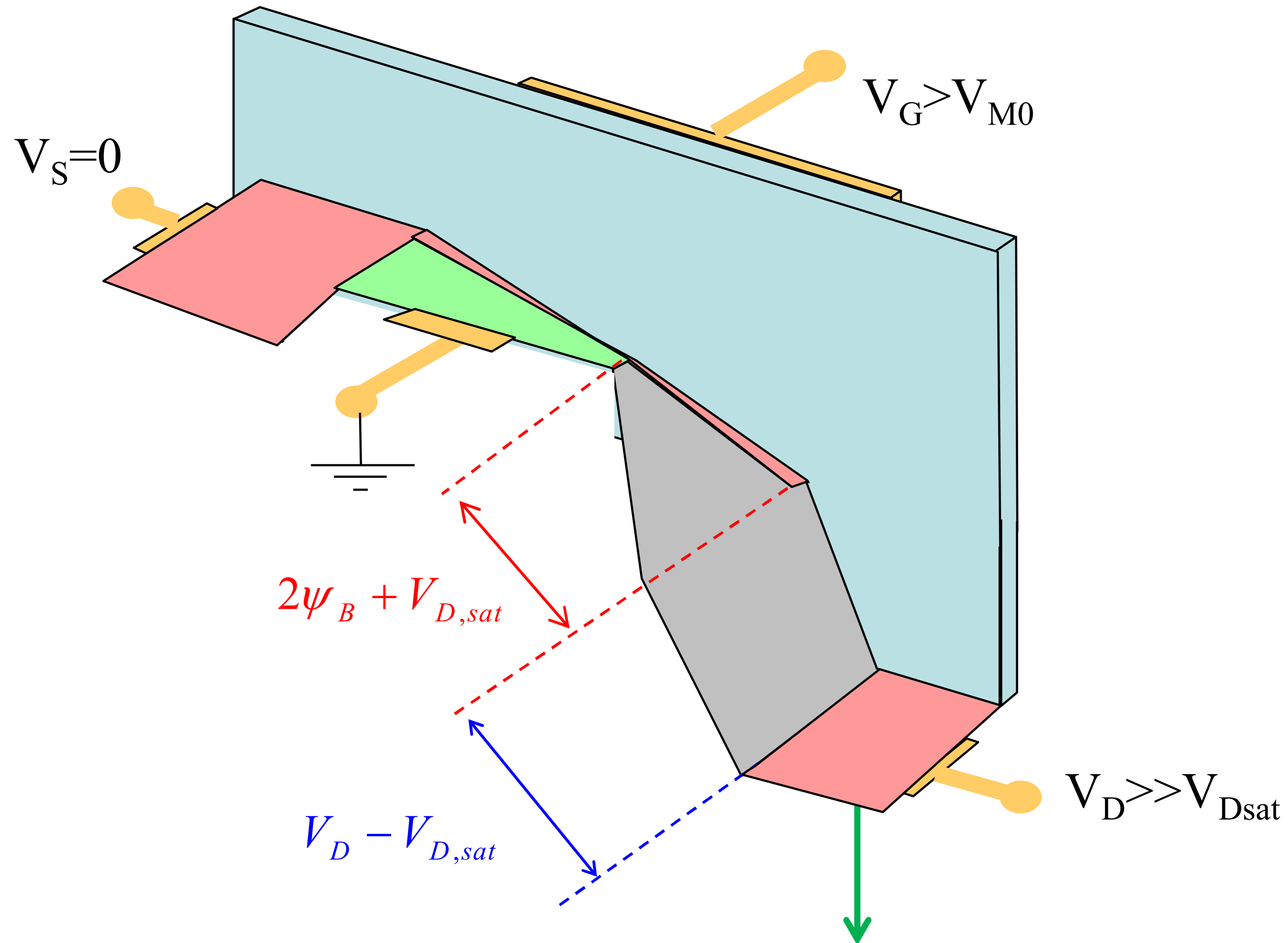
Bande de conduction:



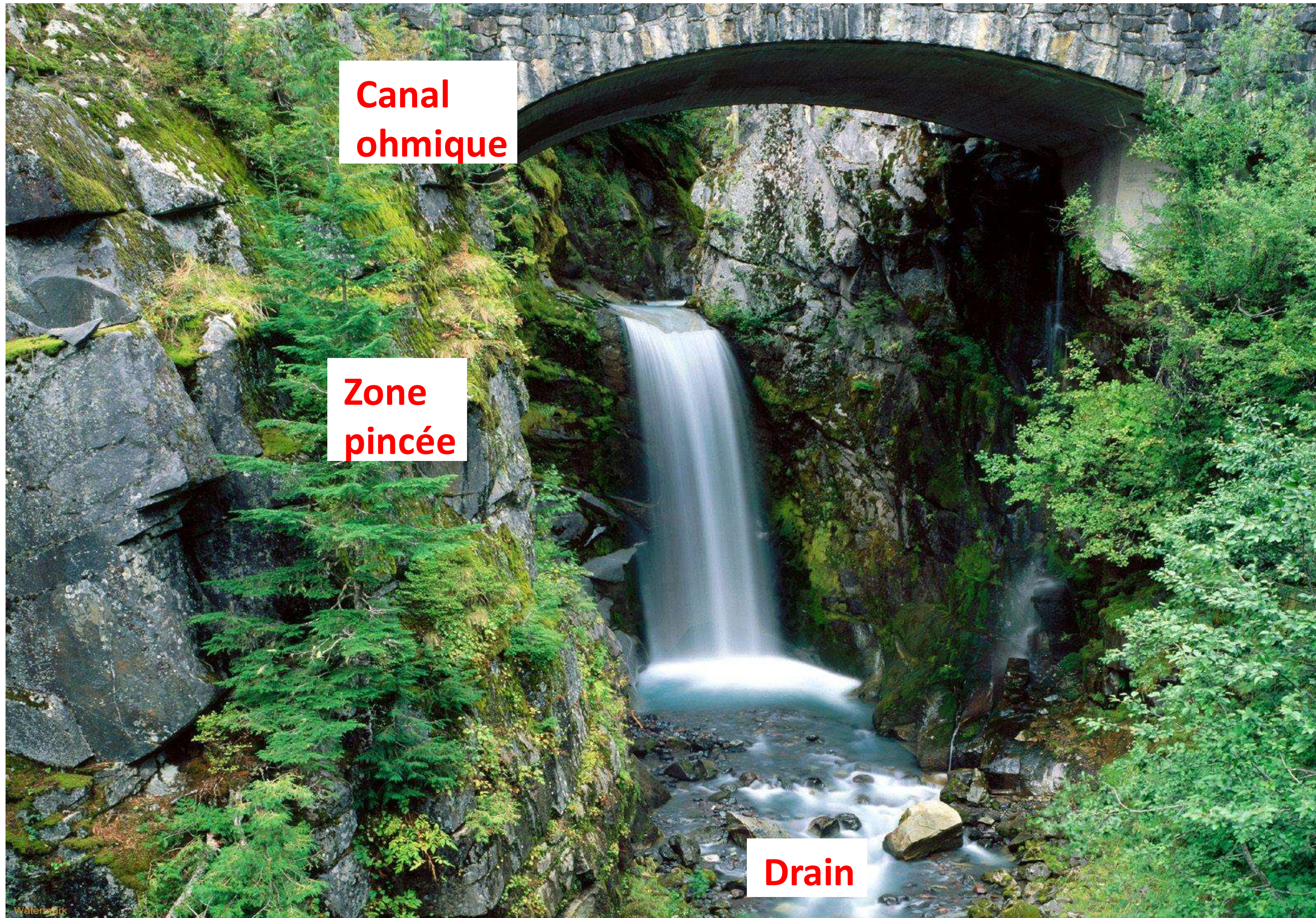
Vue latérale:



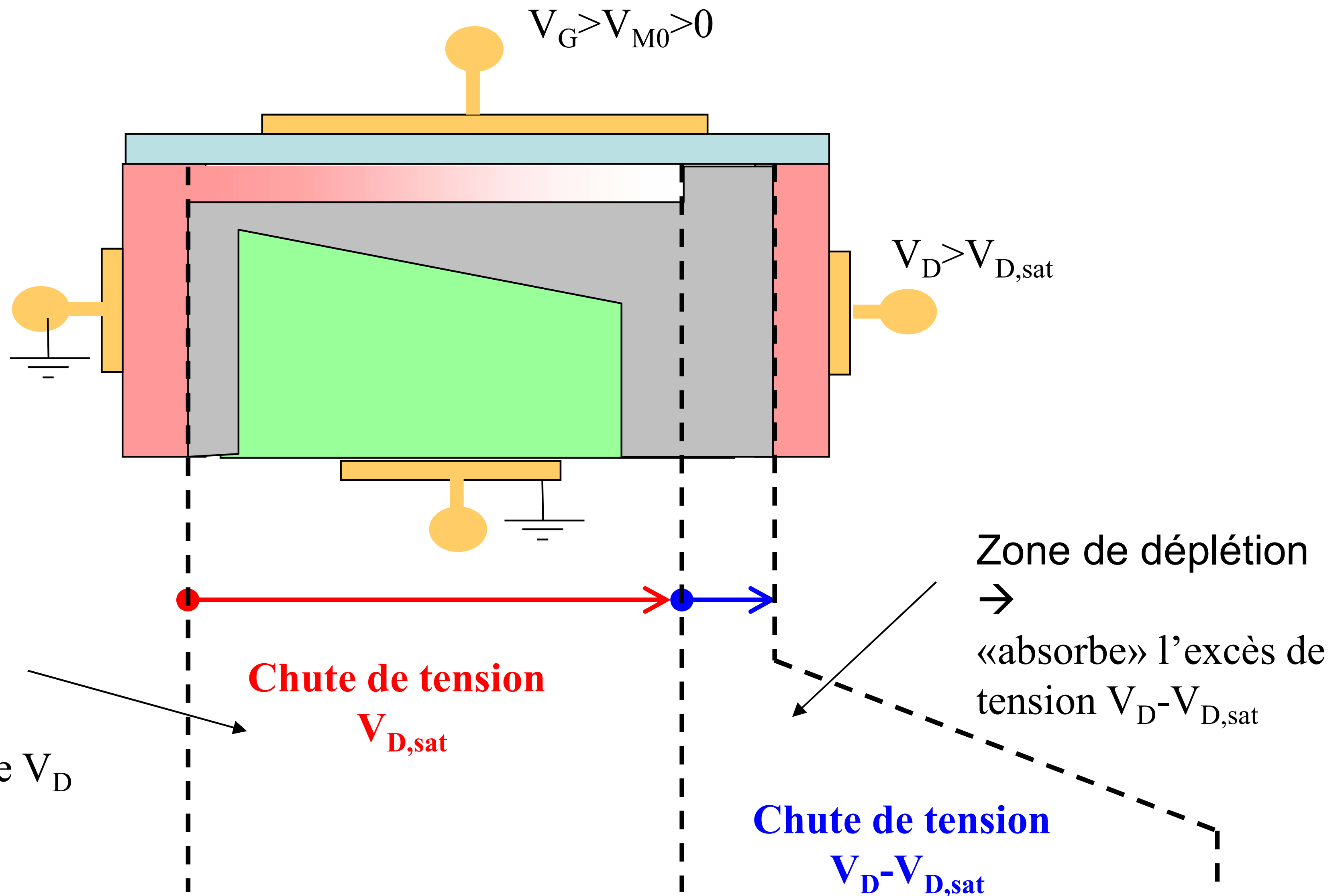
Régime de saturation



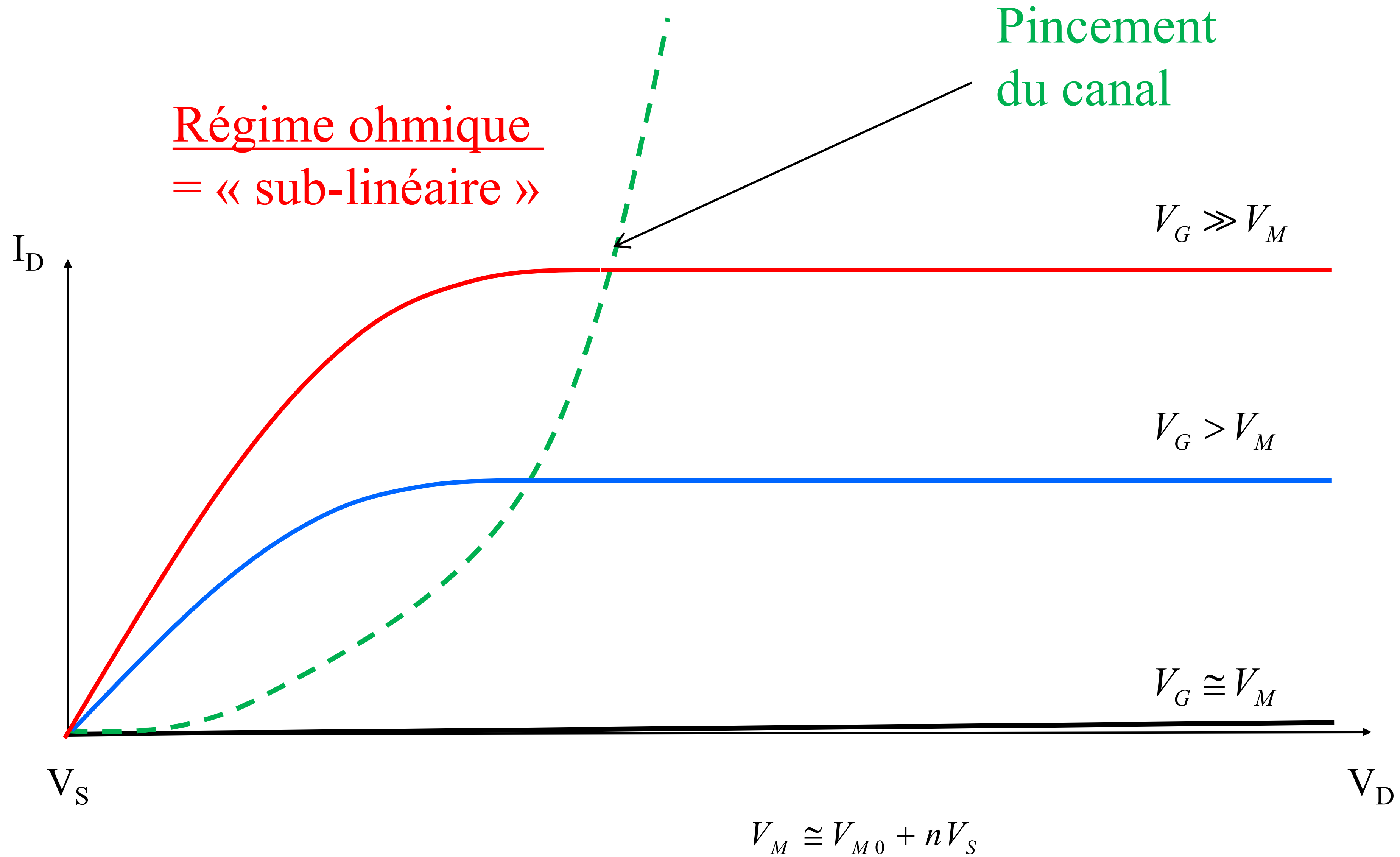
Pincement du canal NMOS



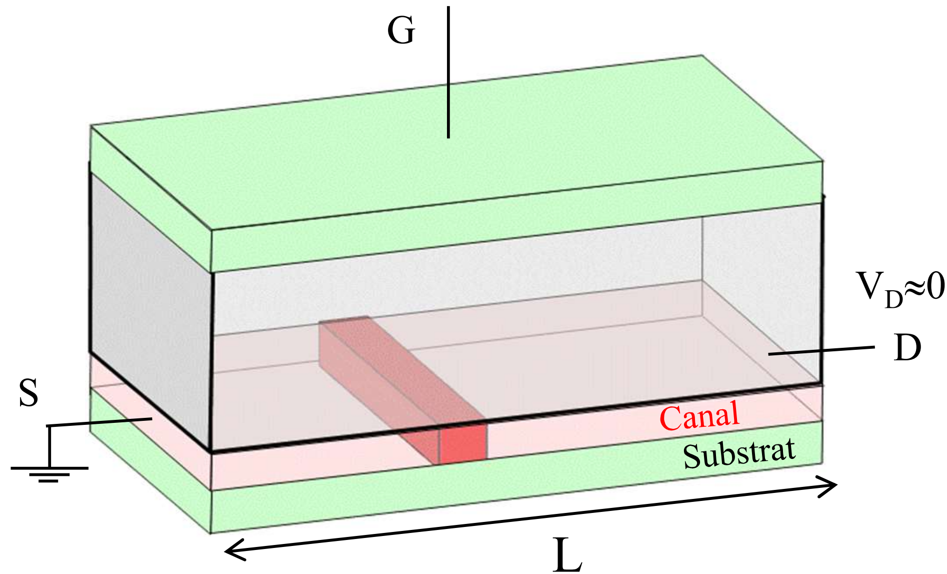
Pincement du canal

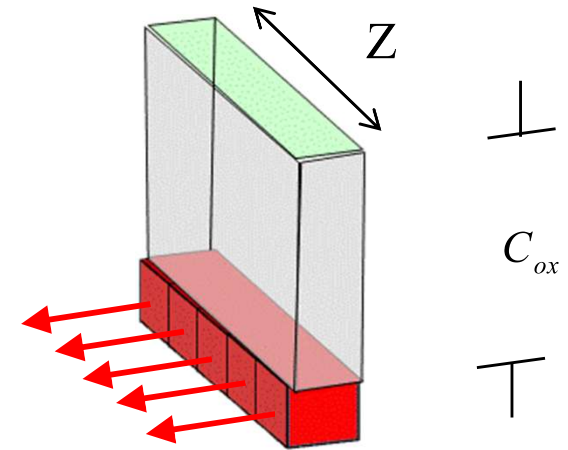


Régime FET idéal



Exercice: calcul simplifié du courant en inversion forte





$$|Q_n| = C_{ox}\,(V_G - V_{M0} - n V_C)$$

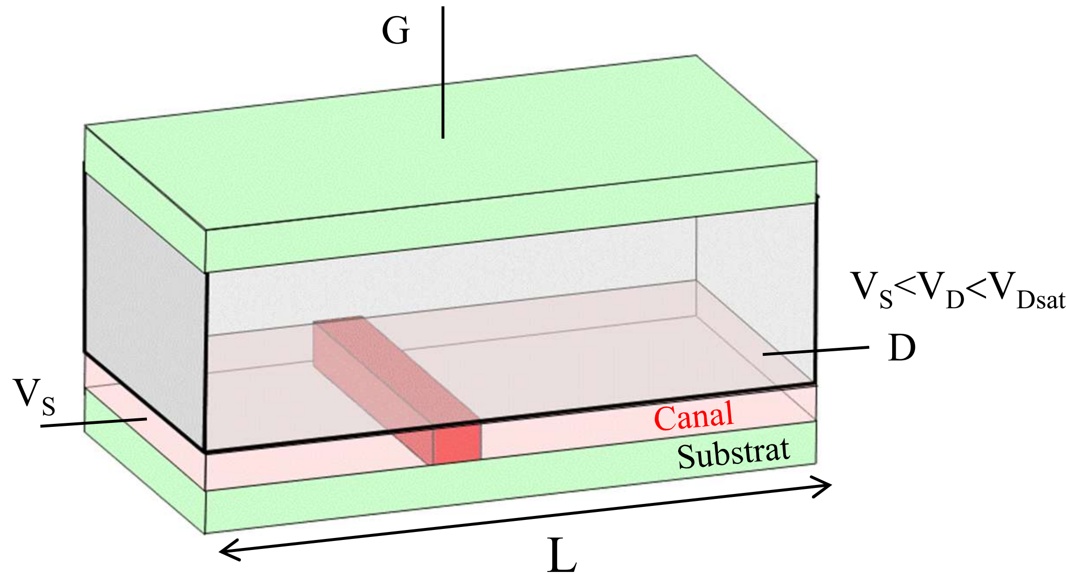
$$\frac{I_D}{Z} = Q_n \,.\, v = \ldots$$

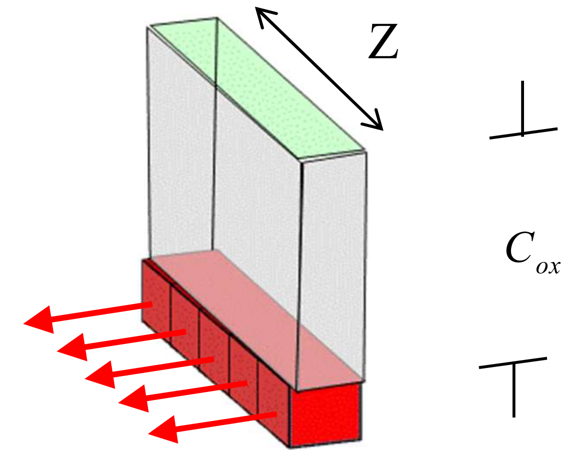
Développez l'expression du courant en considérant la charge et la vitesse moyenne au milieu du canal

PAB

Exercice: calcul simplifié du courant en inversion forte

A) Régime ohmique





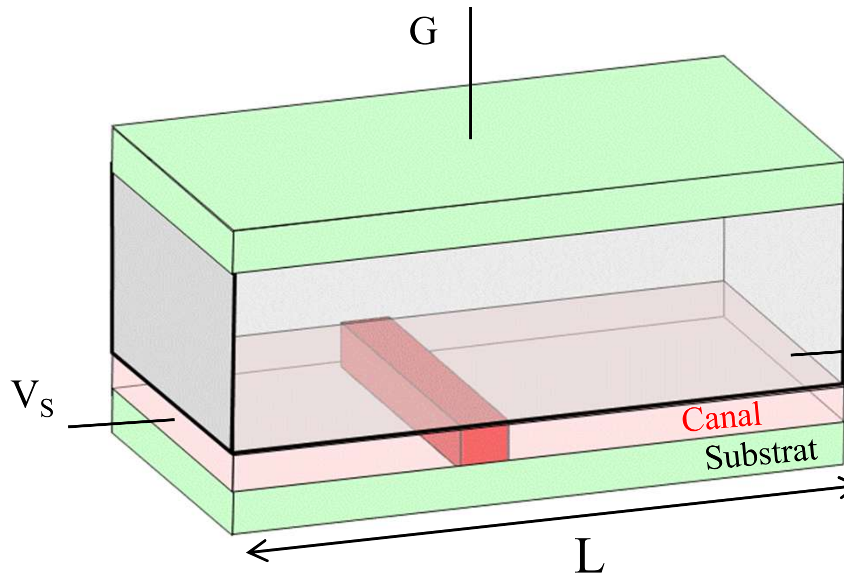
$$|Q_n| = C_{ox}\,(V_G - V_{M0} - n V_C)$$

$$\frac{I_D}{Z} = \left(\frac{Q_{n,S}+Q_{n,D}}{2}\right)\cdot\left(\mu_n \left|\vec{E}\right|\right) = C_{ox}\left(V_G - V_{M0} - n\frac{V_D+V_S}{2}\right)\cdot\left(\mu_n \frac{V_D - V_S}{L}\right)$$

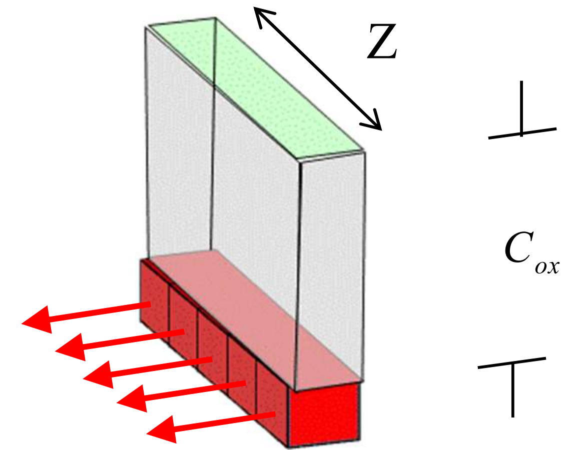
PAB

Exercice: calcul simplifié du courant en inversion forte

B) Régime de saturation



$$V_{Dsat} = \frac{V_G - V_{M0}}{n}$$



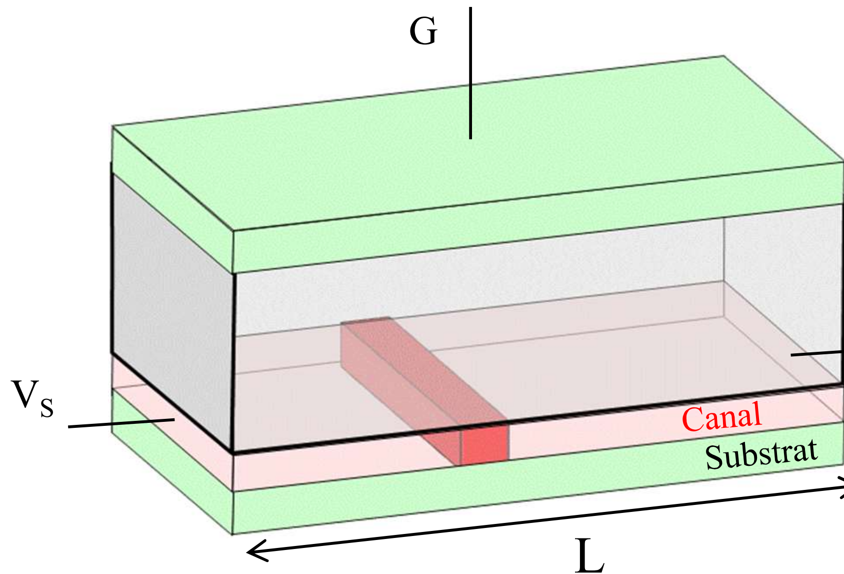
$$|Q_n| = C_{ox}\,(V_G - V_{M0} - nV_C)$$

$$\frac{I_D}{Z} = \left(\frac{Q_{n,S} + Q_{n,D}}{2}\right)\cdot\left(\mu_n\left|\vec{E}\right|\right) = \frac{C_{ox}\left(V_G - V_{M0} - nV_S\right)}{2}\cdot\left(\mu_n\frac{V_{D,sat} - V_S}{L}\right)$$

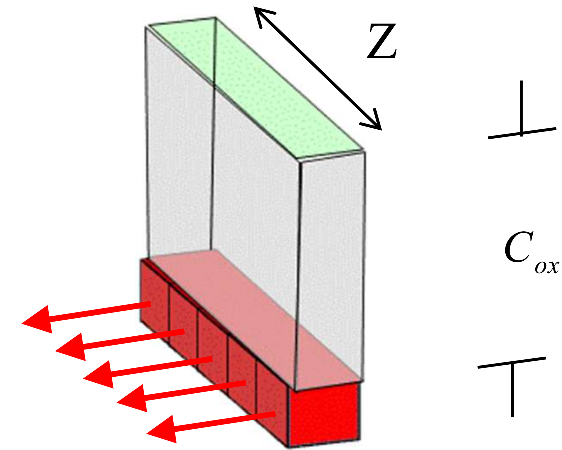
($Q_{n,D} \rightarrow 0$)

Exercice: calcul simplifié du courant en inversion forte

B) Régime de saturation



$$V_{Dsat} = \frac{V_G - V_{M0}}{n}$$



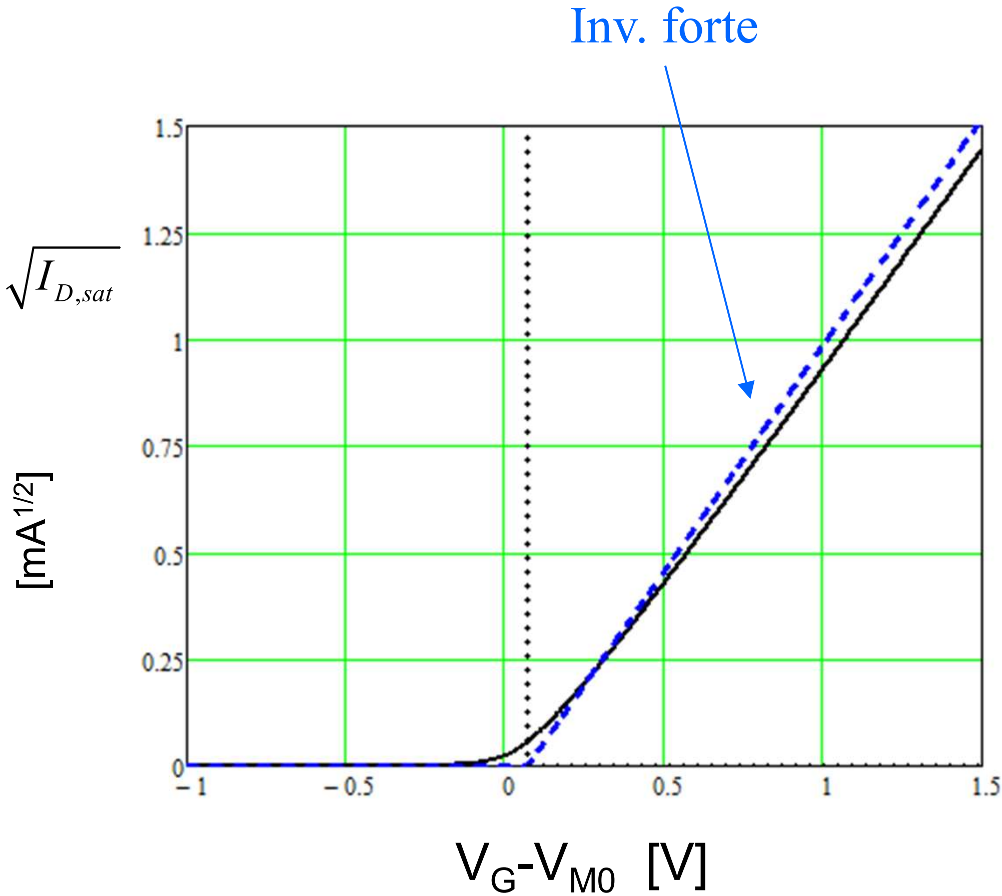
$$|Q_n| = C_{ox}\,(V_G - V_{M0} - nV_C)$$

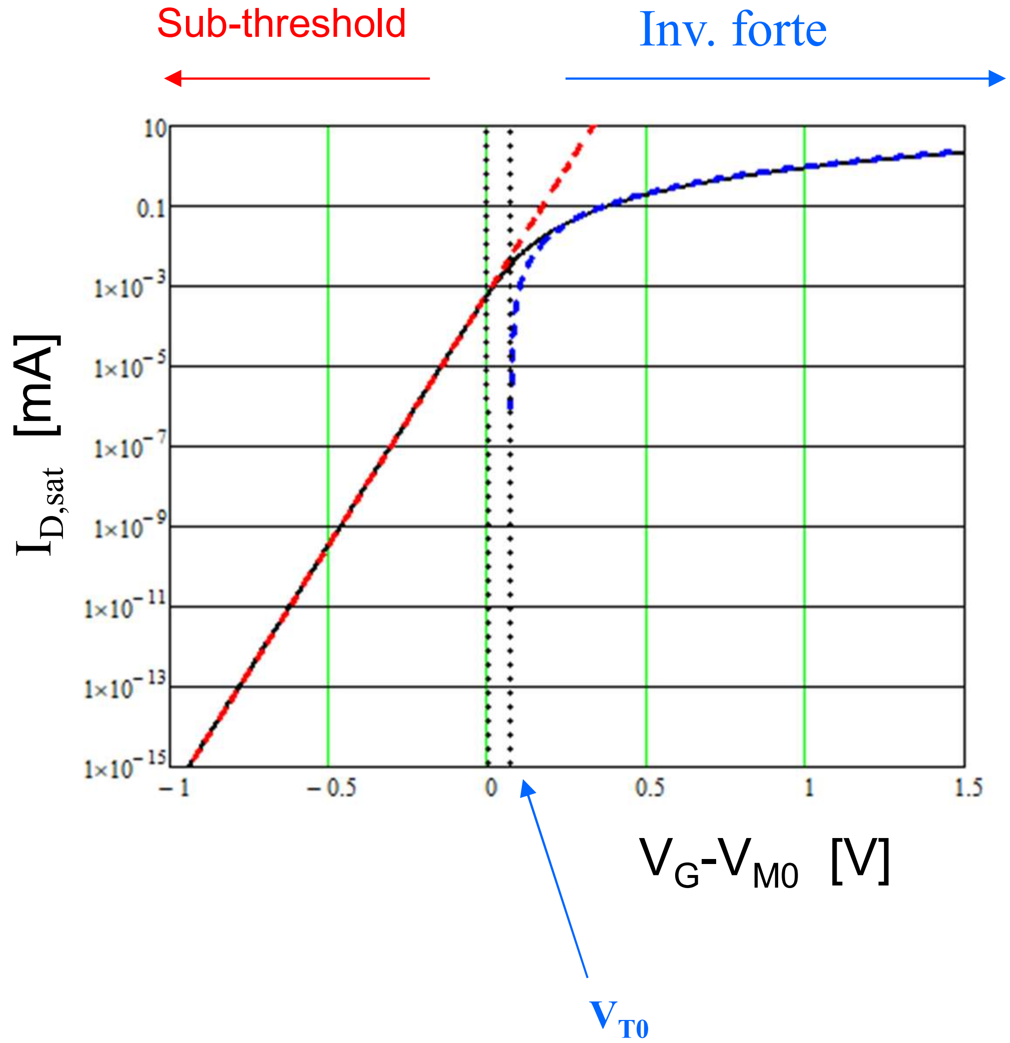
$$I_D = Z\left(\frac{Q_{n,S} + Q_{n,D}}{2}\right)\cdot\left(\mu_n\left|\vec{E}\right|\right) \quad = \frac{1}{2\cdot n}\cdot\frac{Z}{L}\cdot\mu_n C_{ox}\cdot\left(V_G - V_{M0} - nV_S\right)^2$$

($Q_{n,D}$ → 0)

PAB

Inversion forte en saturation ($V_D > V_{D,sat}$)



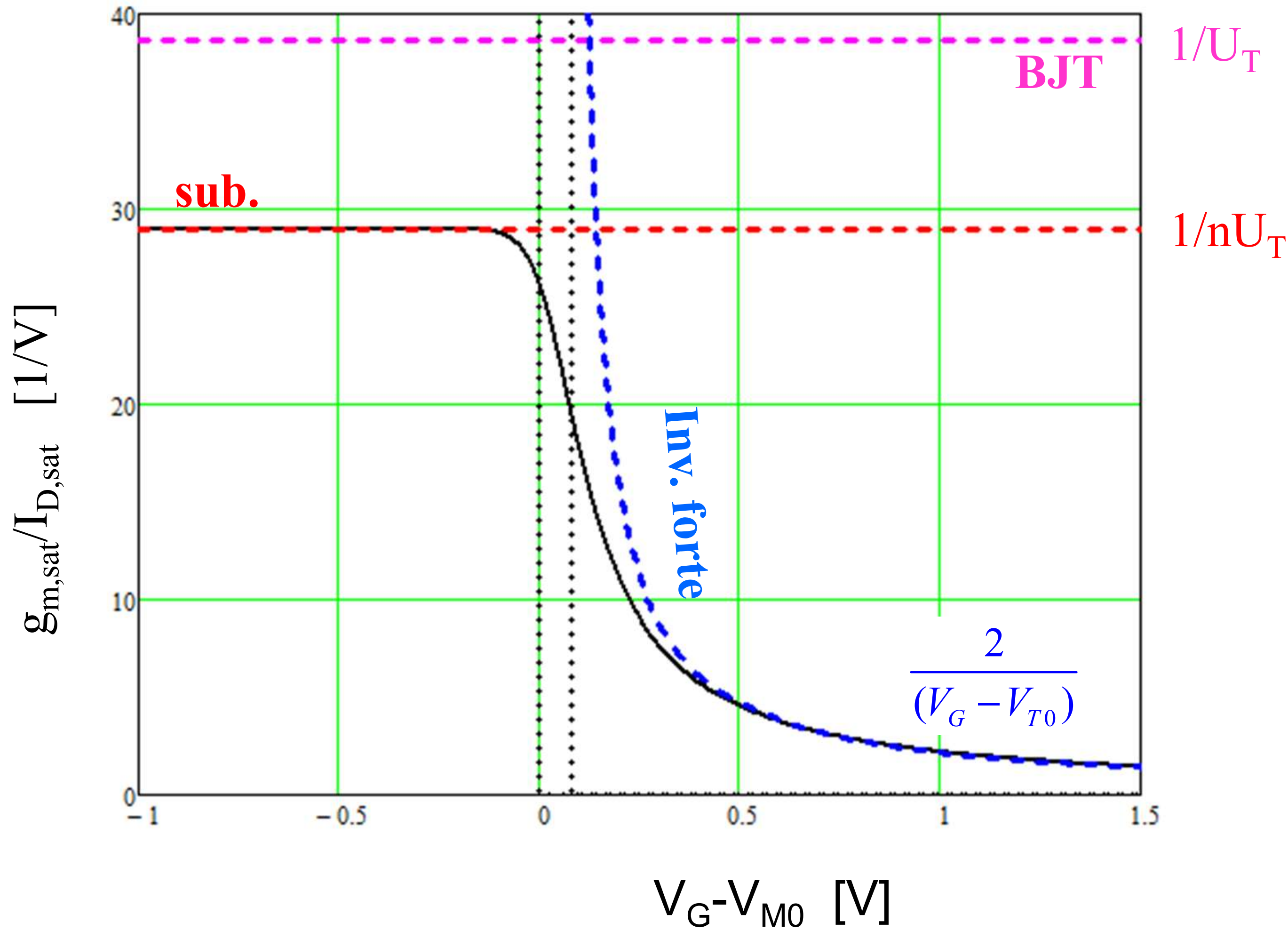


C_{ox}=3fF/um^2
W/L=10
T=300 K

u_n=1000cm^2/V.s
n=4/3

PAB

Transconductance en saturation: g_m/I_D



Transconductance définition

$$g_{m,sat} \equiv \frac{\partial I_{D,sat}}{\partial V_G}$$

C_{ox}=3fF/um^2
W/L=10
T=300 K

u_n=1000cm^2/V.s
n=4/3

Résumé NMOS : comportement en régime FET en fonction de la tension de drain

I_D

$V_G \gg V_M$

$V_G > V_M$

$V_G \cong V_M$

A

B

C

D

$V_{DS,sat}$

V_{DS}

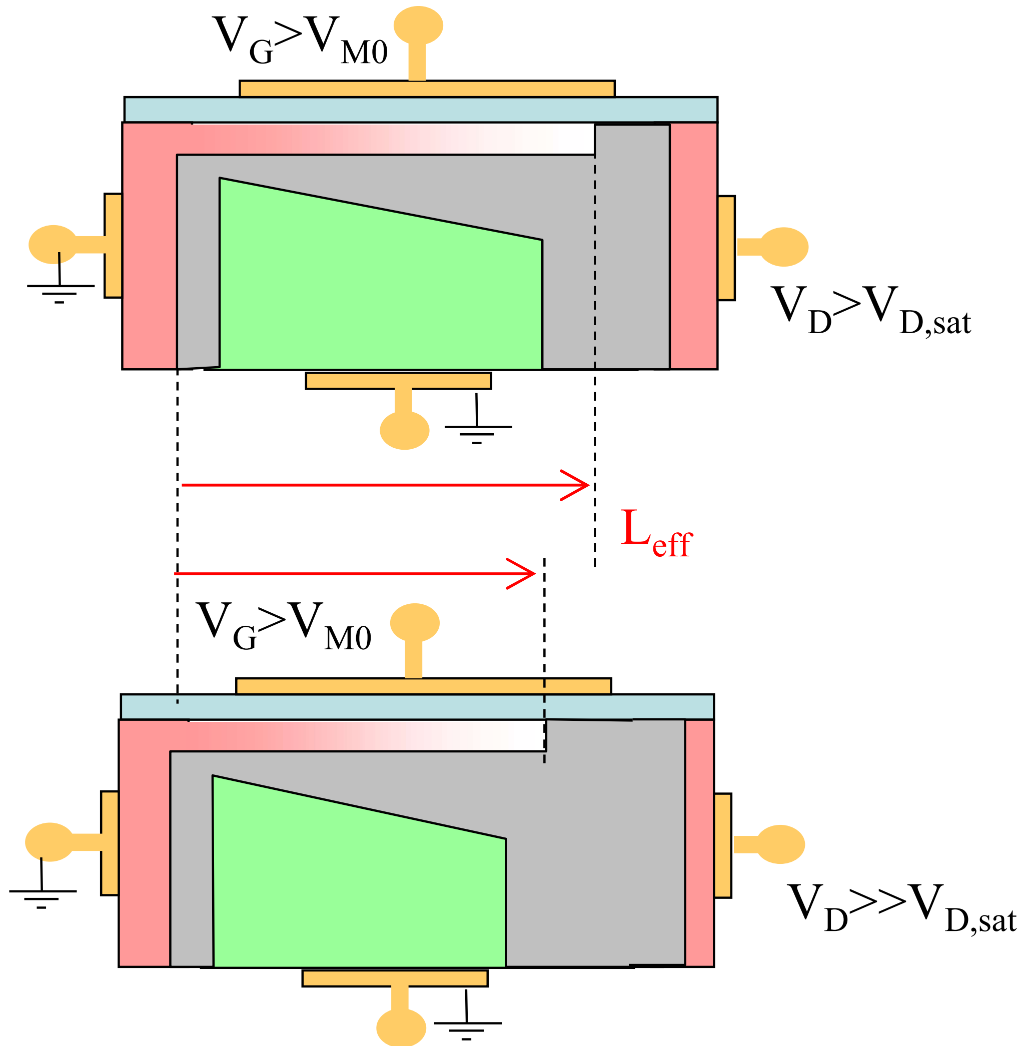
Résumé NMOS (1)

A)

B)

Résumé NMOS (2)

Modulation de la longueur du canal



Le canal se rétrécit lentement avec l'augmentation de la tension de drain V_D.

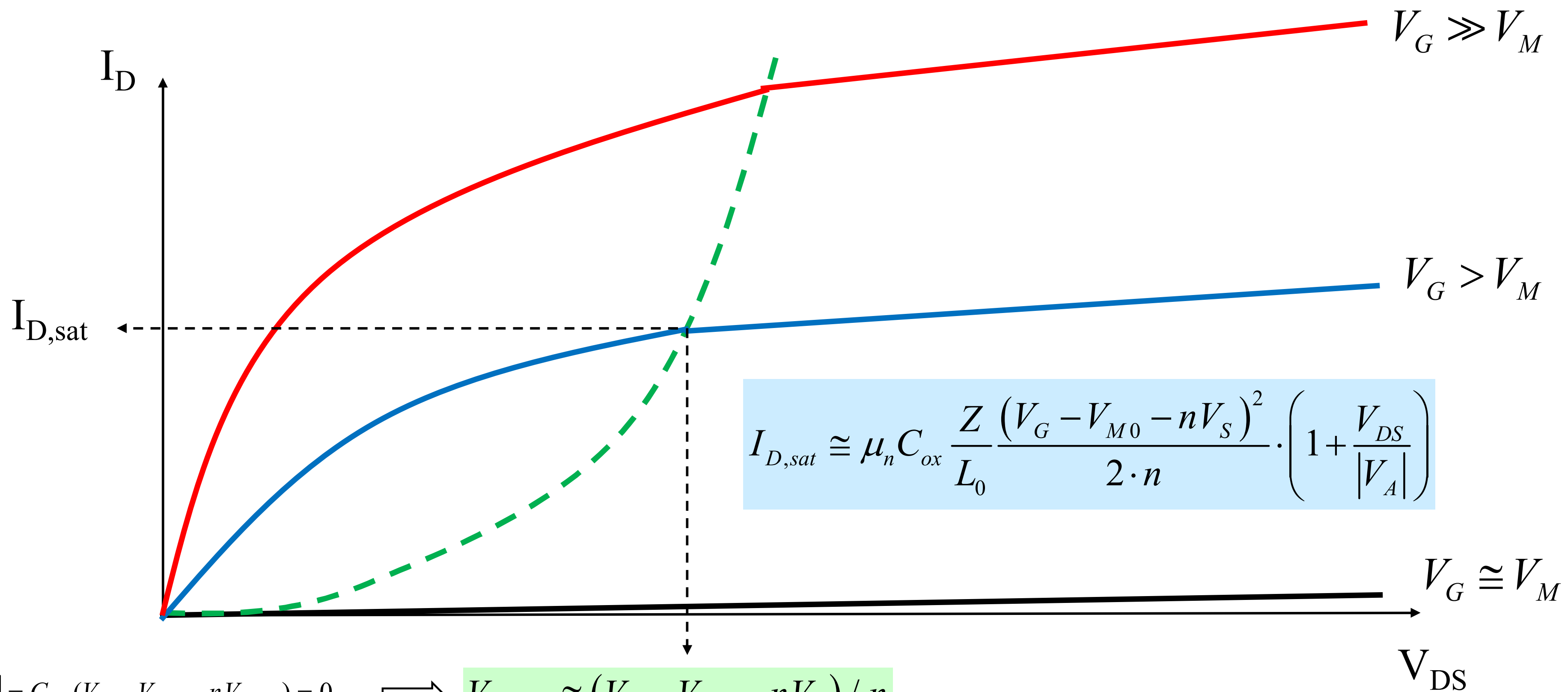
→ Le courant de drain augmente légèrement

$$I_{D,sat} \approx \frac{1}{L_{eff}} = \frac{1}{L_0} \cdot \left(1 + \frac{V_{DS}}{|V_A|}\right)$$

PAB

Courbes de sortie en mode FET avec modulation de la longueur du canal

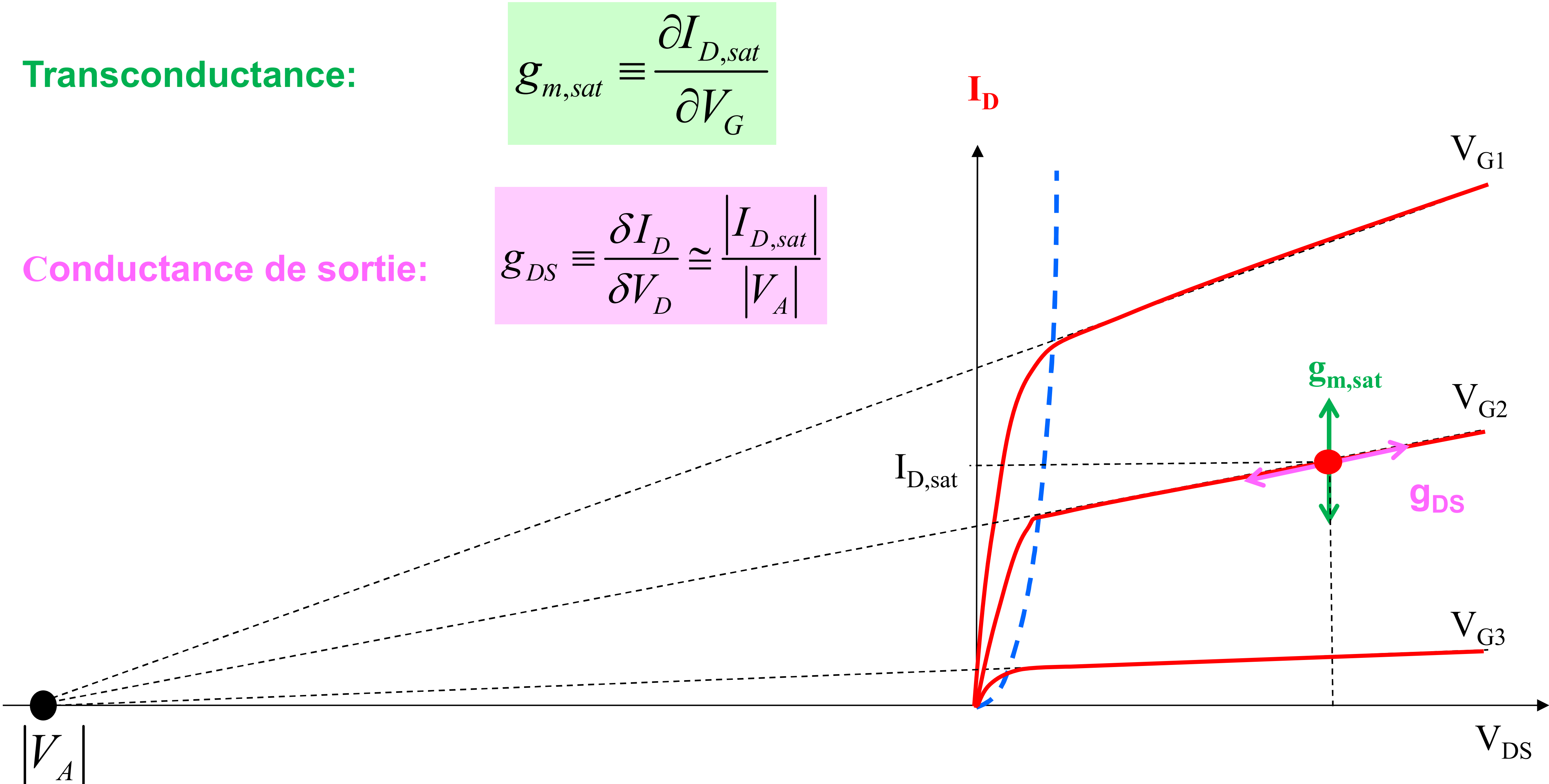
$$\frac{g_{m,sat}}{I_{D,sat}} \equiv \frac{1}{I_{D,sat}}\frac{\partial I_{D,sat}}{\partial V_G} \cong \frac{2}{(V_G - V_{M0} - nV_S)}$$



$$|Q_{n,D}| = C_{ox}\,(V_G - V_{M0} - nV_{D,sat}) = 0 \quad \Longrightarrow \quad V_{DS,sat} \cong (V_G - V_{M0} - nV_S)/n$$

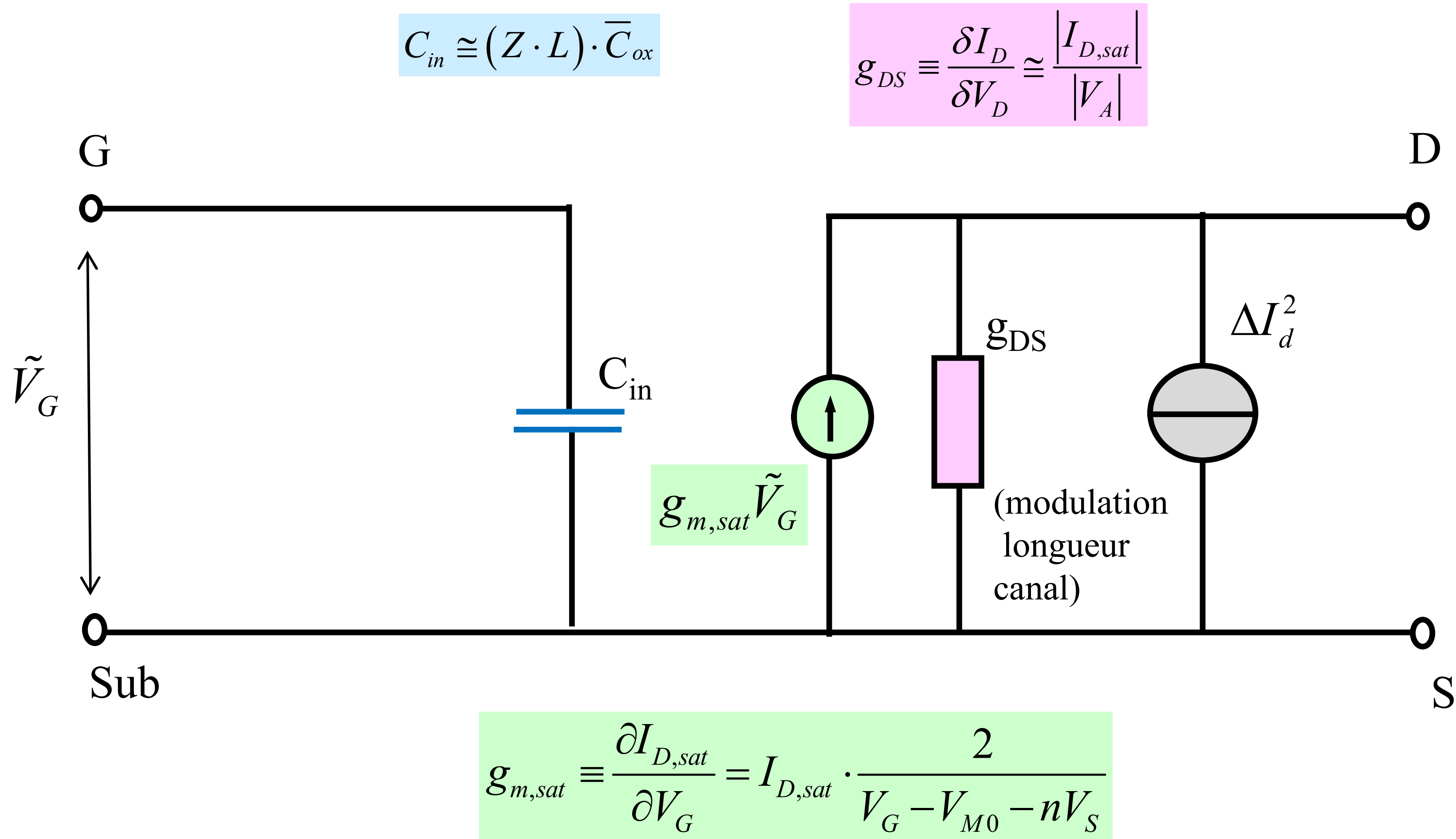
PAB

10.5: circuit petit signaux : Conductances en mode actif

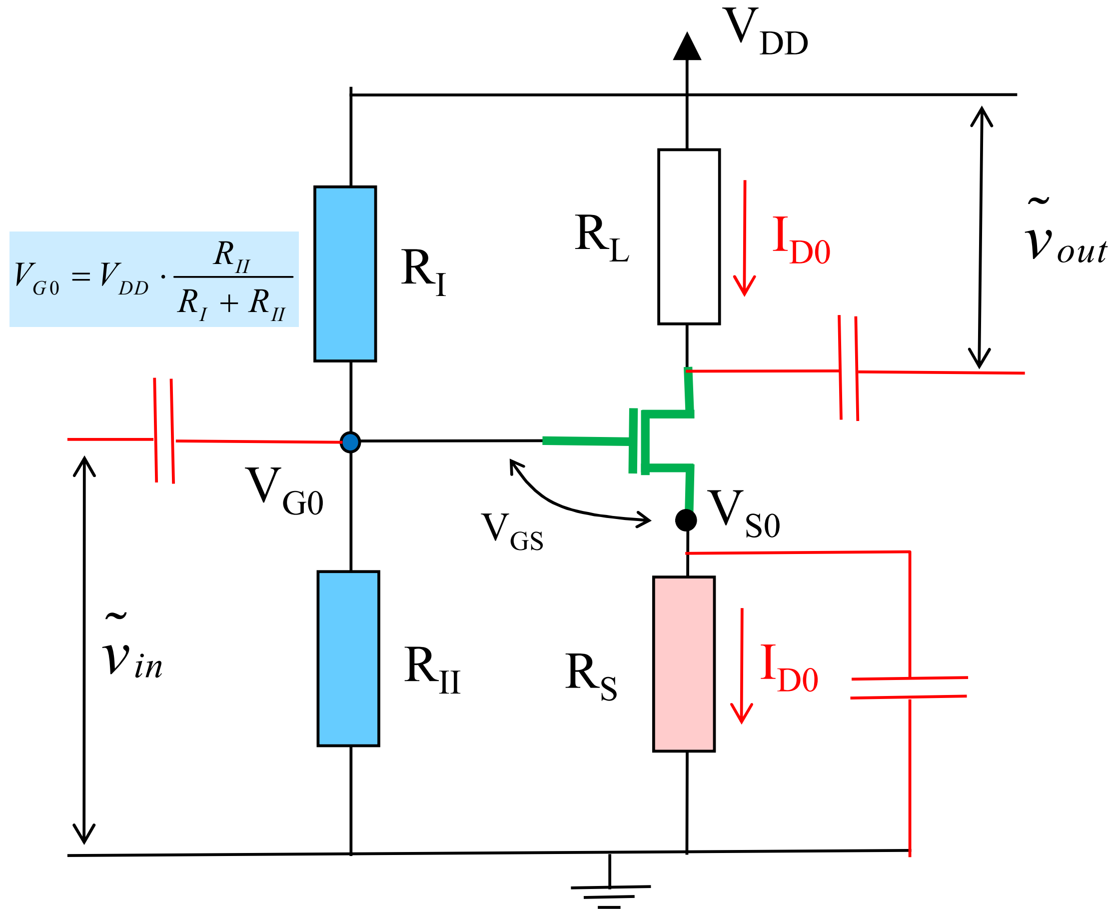


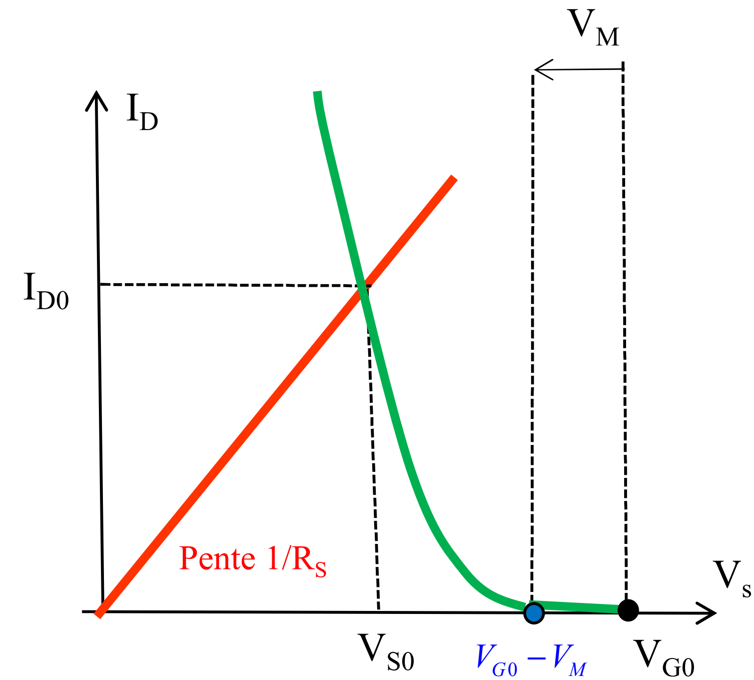
PAB

Circuit petits signaux simplifié



Polarisation du NMOS: point de travail

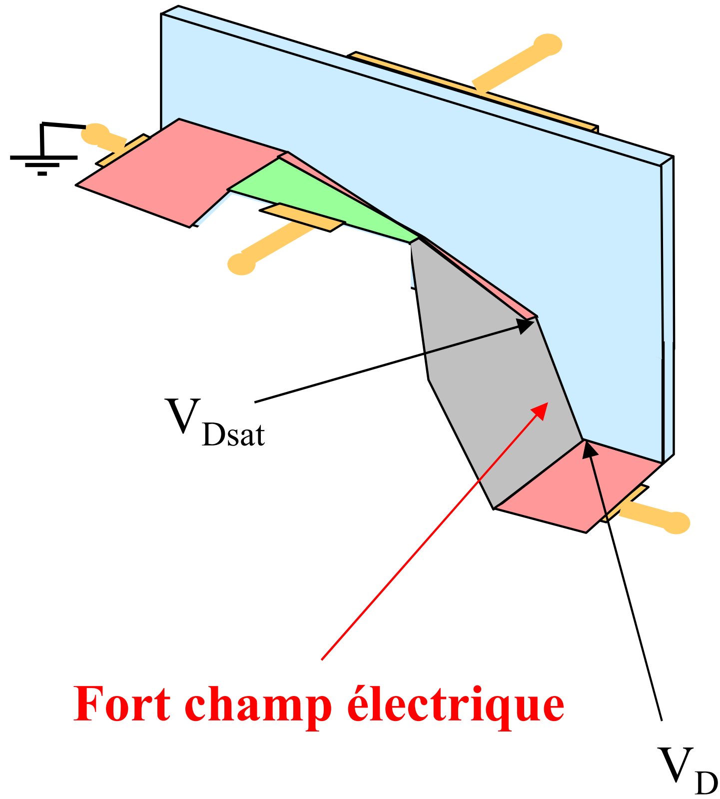




Entrée sur la capacité de gate
→ R_{in} infinie pour ω=0.

Avalanche breakdown

NMOS



10.6: Modèle EKV du NMOS
(voir vidéos complémentaires sur le drive)

Threshold:

$$V_{T0} \equiv V_{fb} + (2n-1)\cdot 2\psi_B + nU_T \ln\left(\frac{2n}{n-1}\right)$$

Normalisation:

$$q_n \equiv \frac{-Q_n}{2nC_{ox}U_T}$$

$$i_D \equiv \frac{-I_D}{2n\cdot \mu C_{ox}\cdot \frac{Z}{L}\cdot U_T^2}$$

Charges:

$$\ln\left(q_{n,S}\right) + 2q_{n,S} \cong \frac{V_G - V_{T0}}{nU_T} - \frac{V_S}{U_T}$$

$$\ln\left(q_{n,D}\right) + 2q_{n,D} \cong \frac{V_G - V_{T0}}{nU_T} - \frac{V_D}{U_T}$$

Courant:

$$i_F \equiv \left(q_{n,S}^2 + q_{n,S}\right) \cong \left[\ln(1+e^{\frac{V_G - V_{T0} - nV_S}{2nU_T}})\right]^2$$

$$i_D = \left(i_F - i_R\right)$$

$$i_R \equiv \left(q_{n,D}^2 + q_{n,D}\right) \cong \left[\ln(1+e^{\frac{V_G - V_{T0} - nV_D}{2nU_T}})\right]^2$$

Transconductance:

$$\frac{g_m}{I_D} = \frac{1}{nU_T}\cdot\frac{1}{\sqrt{\frac{1}{4}+i_F}+\sqrt{\frac{1}{4}+i_R}}$$

Sub-threshold **Strong inversion**

Courant de drain: Modèle EKV

V_S=0 [V] V_{M0}=0.976 V V_{T0}=1.047 V

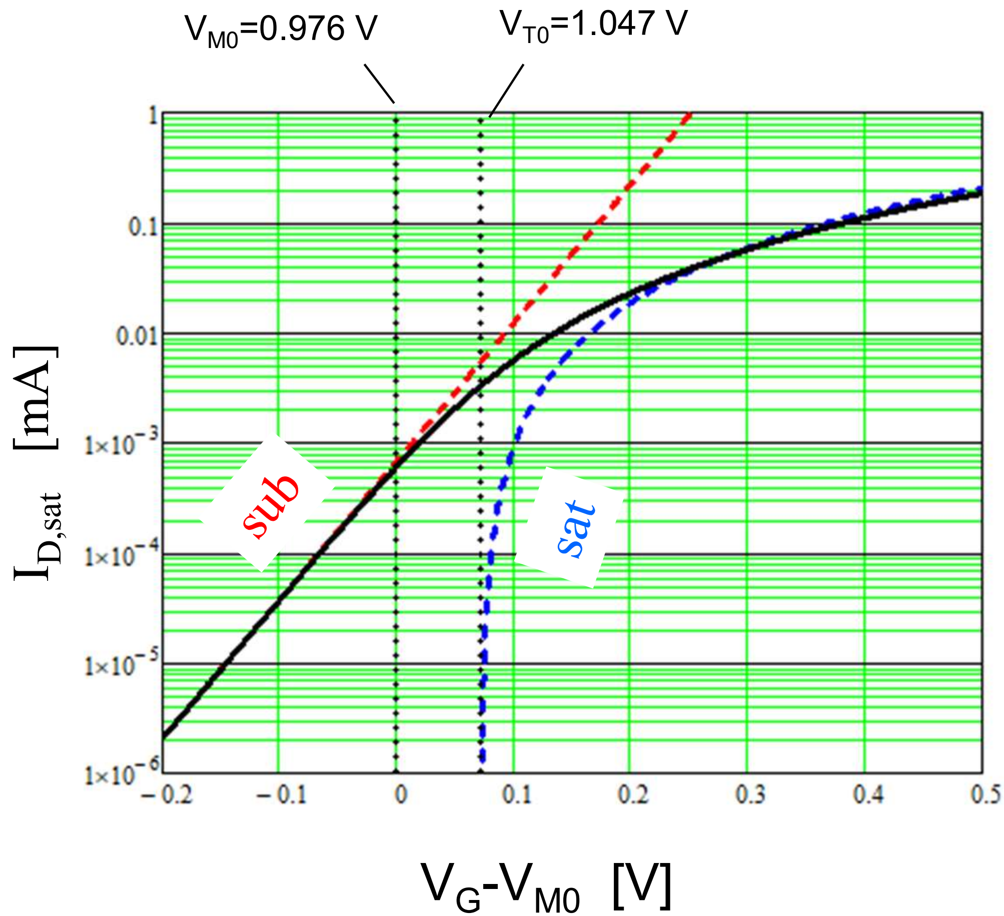
V_G=

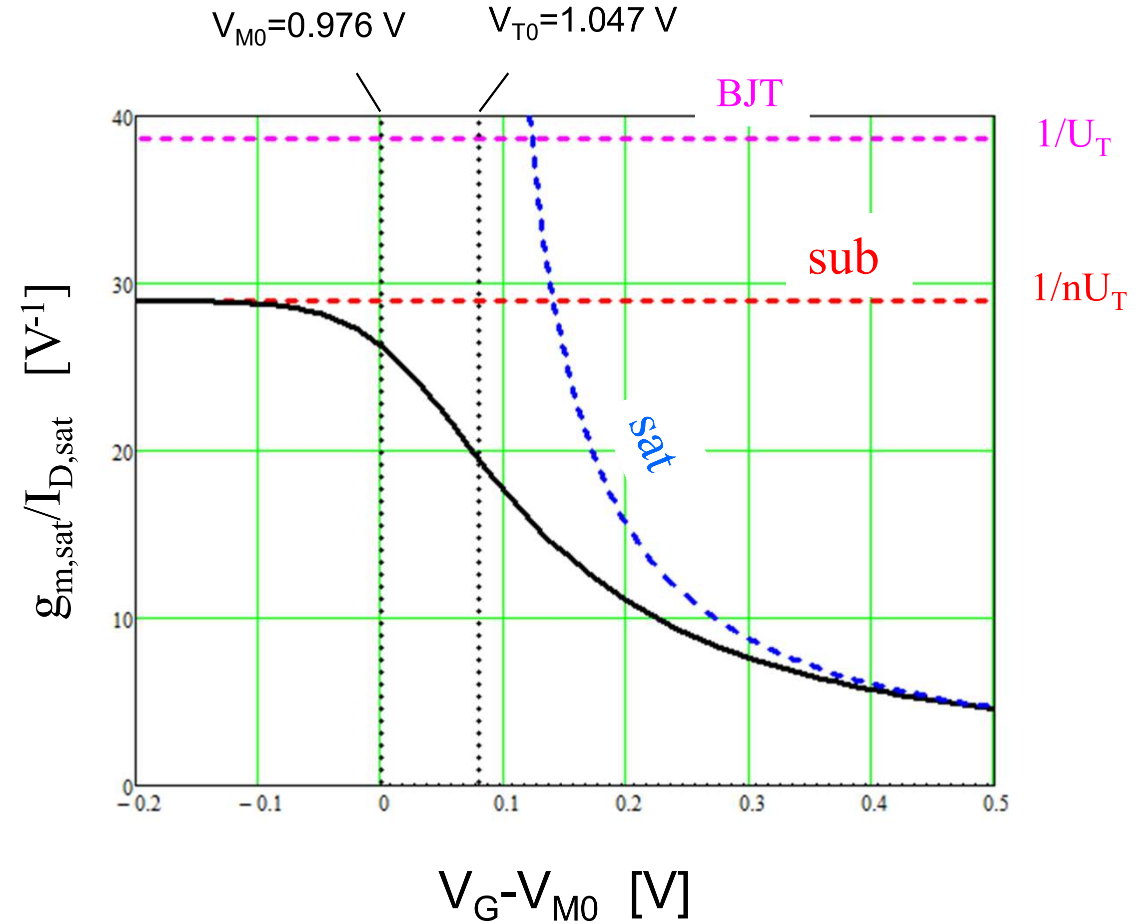
V_G	Régime
3.0 V … 1.4 V	**Inversion forte** — Quadratique
1.2 V, 1.0 V	**Inversion modérée**
0.8 V, 0.6 V, 0.4 V	**Inversion faible «sub-threshold»** — Exponentiel BJT

Courant de drain [mA] (axe logarithmique : 10, 1, 0.1, 0.01, 1×10^{-3} … 1×10^{-11})

Tension de drain V_D [V] (0, 1, 2, 3, 4)

Comparaison des modèles





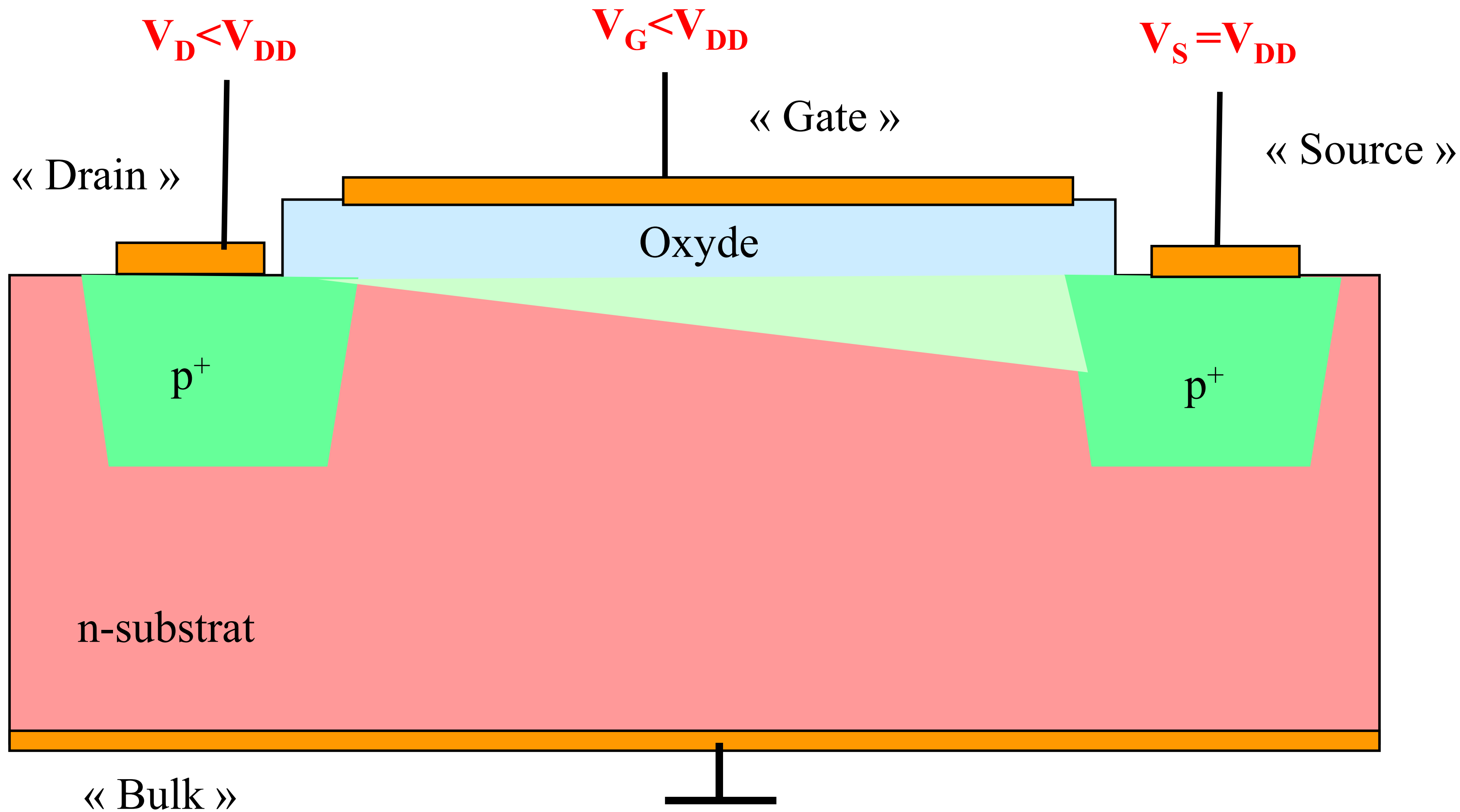
C_{ox}=3fF/um²
W/L=10
T=300 K

u_n=1000cm²/V.s
n=4/3

PMOS: MOSFET à canal P

Le drain et le gate sont à des tensions inférieures au bulk

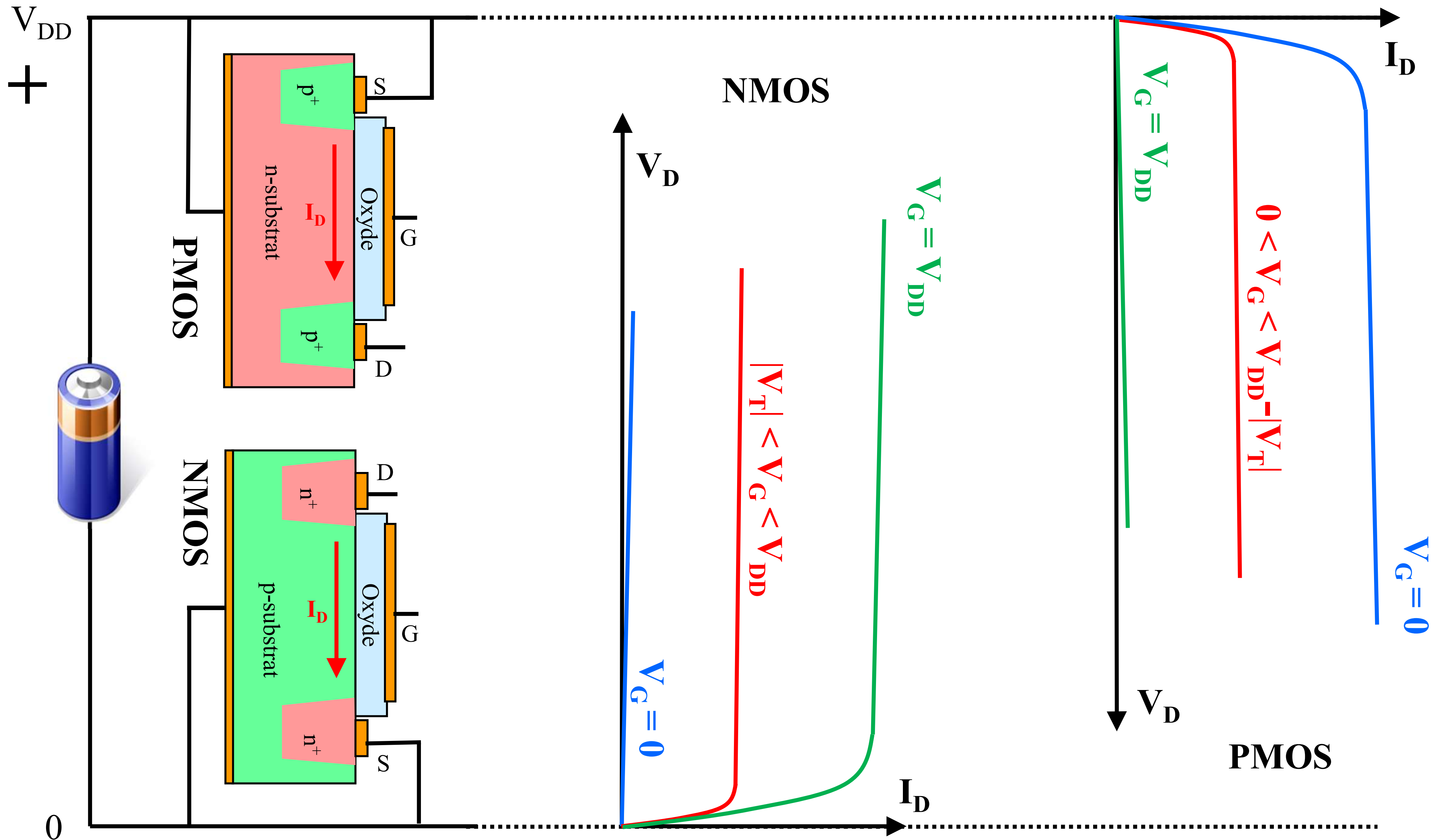
La source est à la tension de bulk



Le bulk est à la tension maximale

PAB

Comparaison NMOS et PMOS: «Complémentarité»



PAB

Exercice E10.2: VLSI et dissipation d’énergie

Considérons un chip avec une “Very Large Scale Integration” (VLSI) travaillant à température ambiante. Il contient 10^9 NMOS, tous “fermés” donc avec une tension de gate V_G=0. Le courant “subthreshold” est exprimé par:

$$I_{D,sub} \cong I_{0,sub} \cdot e^{q(V_G - V_T)/nkT} \quad avec \quad n = 1.33$$

A) Le courant à V_G=0 V pour une tension de threshold V_T=0.5 V est de 4 pA par transistor. Quelle est la consommation en courant de tout le chip lorsque les transistors sont tous fermés ?

B) Nous diminuons la tension de threshold à V_T=0.25V. Quelle est maintenant la consommation en courant de tout le chip lorsque les transistors sont tous fermés ?

<u>Commentaire:</u> Cet exercice vise à montrer que le courant “subthreshold” pose une limite inférieure pour la tension de voltage, ceci afin d’assurer une bonne “fermeture” des transistors. Dans un micro-processeur, il y a en effet beaucoup plus de transistors au repos que de transistors “ouverts”.

Exercice E10.3: question de réflexion

Répondez à la question de réflexion

	Quelles sont les contraintes sur l'oxyde d'une structure MOS ? Discutez le cas d'une structure MOS sur substrat p en inversion forte (transistor) et celui de la même structure en déplétion profonde (CCD).

Exemple: on applique 5V sur le gate. Dans lequel des deux cas (inversion forte ou déplétion profonde) le champ électrique dans l'oxyde est-il le plus important ? (risque de claquage!).

Exercices E10.4

E10.4: MOSFET avec grille et drain court-circuités

a) Lorsque la tension de drain et celle de gate sont court-circuitées ($V_G = V_D$), comparez la tension de drain V_D avec la tension de saturation $V_{D,sat}$. (nous supposons une tension de threshold V_{M0} positive pour le NMOS, et la source et substrat connectés à la masse)

b) Que peut-on en déduire sur le régime de fonctionnement du NMOS ?

c) Déterminez la relation courant-tension de ce transistor NMOS avec la grille et le drain court-circuités.

d) Comment peut-on à partir de la mesure de cette caractéristique déterminer la tension de seuil ?